ELEC 5250/6250 – Homework Project 3 – Verilog Simulations
(Due dates for Parts 1 and 2 on course web page.)

You are to perform four simulations of the modulo-6 counter designed previously. Your tests should be designed to fully verify the functionality of the counter, as discussed in class.

(A recorded Modelsim tutorial/demonstration is available in the Canvas Files menu)

Part 1:

1. Simulate the dataflow model, using a "do file" (macro file).
2. Simulate the behavioral model, using the same "do file".

Part 2:

1. Simulate the dataflow model, using a testbench.
2. Simulate the behavioral model, using the same testbench.

For each, generate a printout of either a "wave" or a "list" window from Modelsim, and **hand-annotate** to show me where in the simulation each of the counter's functions is verified (clear, count, load). You need to convince me that all functions have been fully verified in the simulation.

Items to submit:

1. Your original schematic from Project 1, with instructor comments.
2. Your dataflow and behavioral Verilog models from Project 2, corrected as necessary.
3. Part 1: A printout of your "do file".
   Part 2: A printout of your testbench.
4. A printout of the two annotated wave or list windows (for each part)