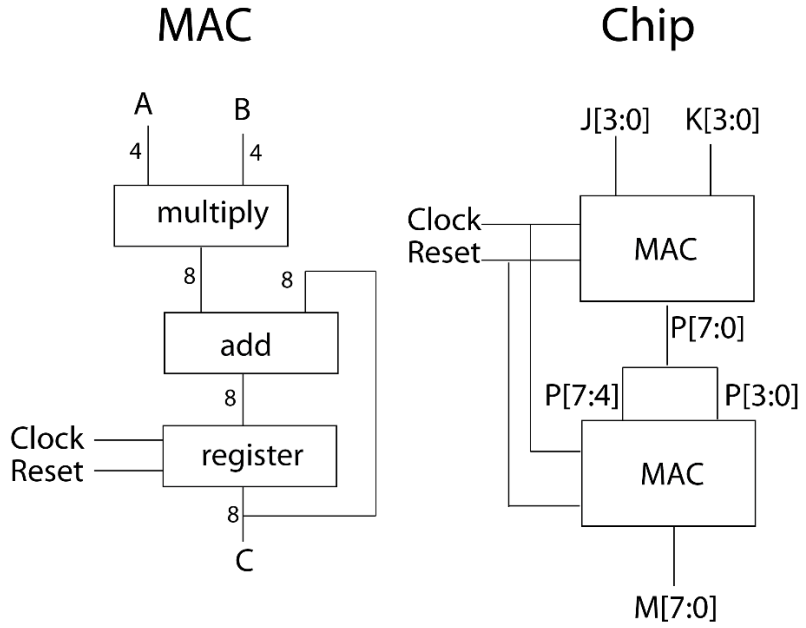
ELEC 6250 – Final Exam/Project – Fall Semester 2018
Due Friday, December 7, by 4:00 p.m.

Since this project serves as the final exam, any form of collaboration with others in the class is prohibited. This is to be an individual effort to demonstrate your knowledge of the subject. Any collaboration and/or duplication of designs or results will be considered a violation of the Academic Honesty Code.

You are to design a "Chip" that contains two registered multiply-accumulate (MAC) blocks, as pictured below, that might be used in digital signal processing applications. The MAC is to perform the operation C = C + (A × B), where A and B are unsigned 4-bit numbers and C is the 8-bit number in the register. The active-high Reset signal should clear the register to all 0s, and the register should capture the adder output at the rising edge of each Clock pulse. The "Chip" is to have two 4-bit inputs, J and K, which are the inputs to the first MAC, one 8-bit output M, which is the output of the second MAC, and the Clock and Reset signals, which go to both MACs. The upper and lower 4-bit nibbles of the first MAC output are to be the A and B inputs, respectively, of the second MAC.



Using the **University of Utah ami06 technology**, the MAC is to be modeled in Verilog, synthesized, and a physical layout created in Encounter. Then a layout block, containing two MAC blocks, is to be created in Virtuoso. Finally, a chip-level layout connecting the two-MAC layout block to a pad frame is to be created in Virtuoso.

The report is to be submitted electronically, addressing the following items.

1. RTL Verilog model of the MAC, including appropriate simulation to demonstrate its correctness. The multiplier and adder to be synthesized from arithmetic + and

* operators; DO NOT design multiplier and adder circuits. (This Verilog model should be relatively short.)
2. Synthesized Verilog netlist for the MAC, with appropriate post-synthesis simulation to demonstrate correct functionality. Timing simulation with the SDF file is not required. However, you should report the estimated block size and maximum clock rate of the synthesized circuit.
3. Physical layout of the MAC, including evidence that there are no geometric or connectivity violations, the size of the layout block, and the maximum clock rate. Compare the size and clock rate to those estimated by Synopsys DC.
4. Virtuoso images of the MAC layout, schematic, and symbol, along with a "clean" Diva DRC report for the MAC layout.
5. Two-MAC schematic diagram and layout, with evidence that there are no DRC errors. Report the final layout size.
6. Chip schematic diagram and layout, comprising the two-MAC block and a pad frame, with evidence of no DRC errors. Report the final chip size.