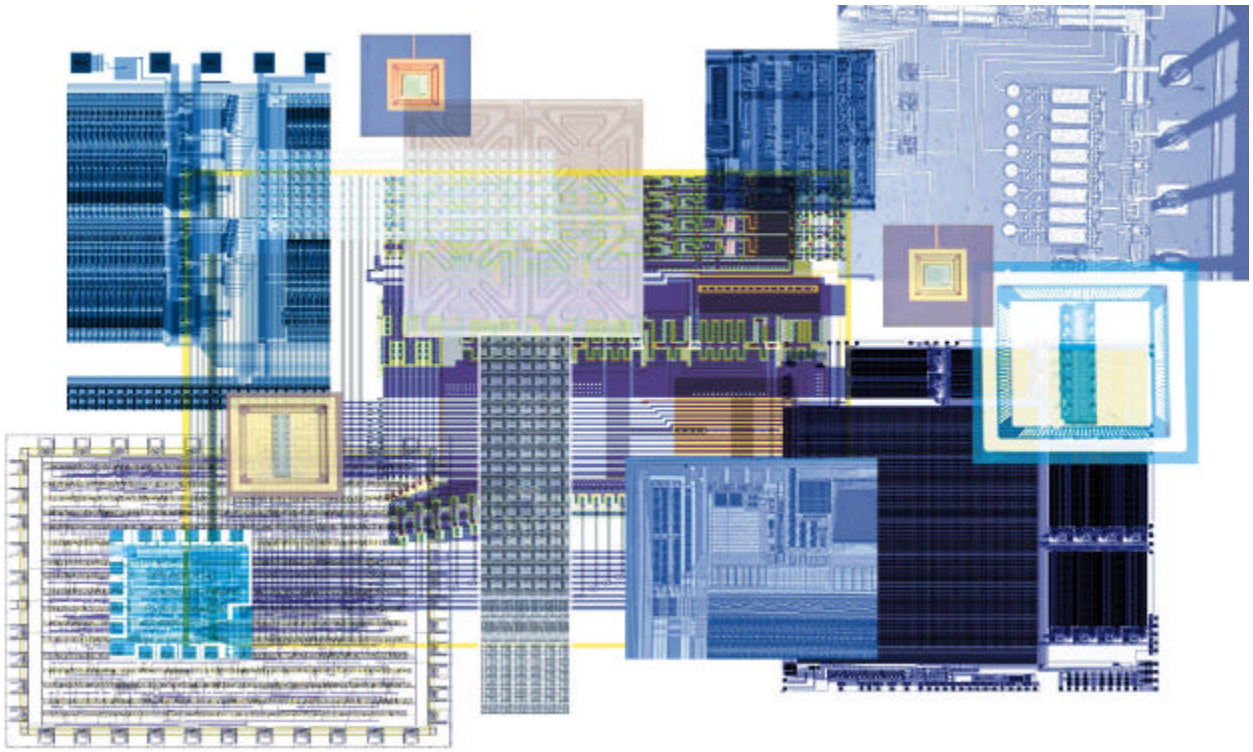
2650 East Foothill Blvd.
Pasadena, CA 91107 USA
Tel: (626) 792-3000
Fax: (626) 792-0300
ces@tanner.com

The MOSIS Service

Hi-ESD Pad Library

TSMC CMOS (0.35µ) Process

June 1999



Tanner Consulting & Engineering Services
develops and delivers advanced ASIC and VLSI solutions for customers.
We accomplish this through training programs, consulting services,
field engineering and contracted design/development efforts.

TANNER CES GENERAL TERMS & CONDITIONS

Liability

All designs will be implemented under the Client's front-end specification. Our contracted engineering services are accomplished for the Client on a best effort basis. Quality assurance is achieved by arriving at a common understanding of the nature of the Project among the engineers and managers at the Client operation and at Tanner CES. Tanner Research is not liable for the functionality, quality, or performance of the Client's future Projects using components produced as part of the contracted work. Tanner Research is not liable if the Client chooses to use our recommended design or application methodologies. If prototype chips are delivered, the process vendors do not generally guarantee yield, quality, or performance of their products. Neither does Tanner Research extend any warrantee to the contracted design and its fabricated results.

Non-Disclosure Agreement

Non-disclosure agreements (NDAs) serve the following purposes.

- Signed between the Client and Tanner Research, the NDA protects Client's original concept, status, and intentions in current and future product development and manufacturing.
- Signed between the Client and Tanner Research, the NDA protects Tanner Research' specific technologies, IC libraries, building blocks and methodologies that are developed prior to the Client Project, or developed specifically for the Client application.
- Specific non-disclosure or non-distribution conditions may be added to the Statement of Work for individual Client Projects. These conditions do not replace or supercede any previously signed NDA; rather they serve as additional constraints to the NDA.
- During or at the end of the Client Project, if we communicate with a process vendor or receive fabricated parts from a process vendor which will be forwarded to the Client, we assume that the Client is also a current customer of the vendor. We may request Client to provide a proof of its NDA with the vendor before any such communication or transaction.

Ownership of Work Results

The Client owns the delivered version and the fabricated version of the work results from a contracted Client Project. These results are subject to the following re-distribution conditions:

- The Client agrees to use the work results only in its own Projects or products, as developed by the Client and on the Client's own site.
- The Client will not distribute copies of the delivered data files and documents (such as design, libraries, process technology setups, design flows and methodologies, software utilities, etc.) to any third parties or to any other Client site, with the following two exceptions:

  Exception 1: If applicable, results can be delivered to the Government Agency sponsoring the Client Project, if such delivery is negotiated as part of the Client Project. During contract negotiations, the Client shall inform Tanner Research about such a delivery and receive advance agreement from us for the contents to be disclosed.

  Exception 2: If applicable, results can be incorporated into published academic research or presented for academic purposes. During contract negotiation, the Client shall inform Tanner Research about such a presentation and receive advanced agreement from us for the contents to be disclosed.

  Any other exceptions shall be specified in a written document signed by both the Client and Tanner Research.

Tanner Research does not own the original design and application concepts from the Client. We agree not to disclose the Client's proprietary design and applications information. However, we shall distinguish the following items that remain the property of Tanner Research:

- The methodology used through the development of the Client Project, or that we planned for Client to apply the Project's results, are usually either common knowledge in the industry or specific methods invented by Tanner Research. Using or adopting these methodologies in the Client Project does not institute the Client's ownership to these methodologies.
- Client does not own Tanner Research's general-purpose building elements (such as cell libraries, building blocks, IO pad cells, etc.) that we utilize in a contracted Project. These building elements are Tanner Research's current design resources that are widely used internally and/or distributed as commercial products. Using these building elements does not institute the Client's ownership of them.

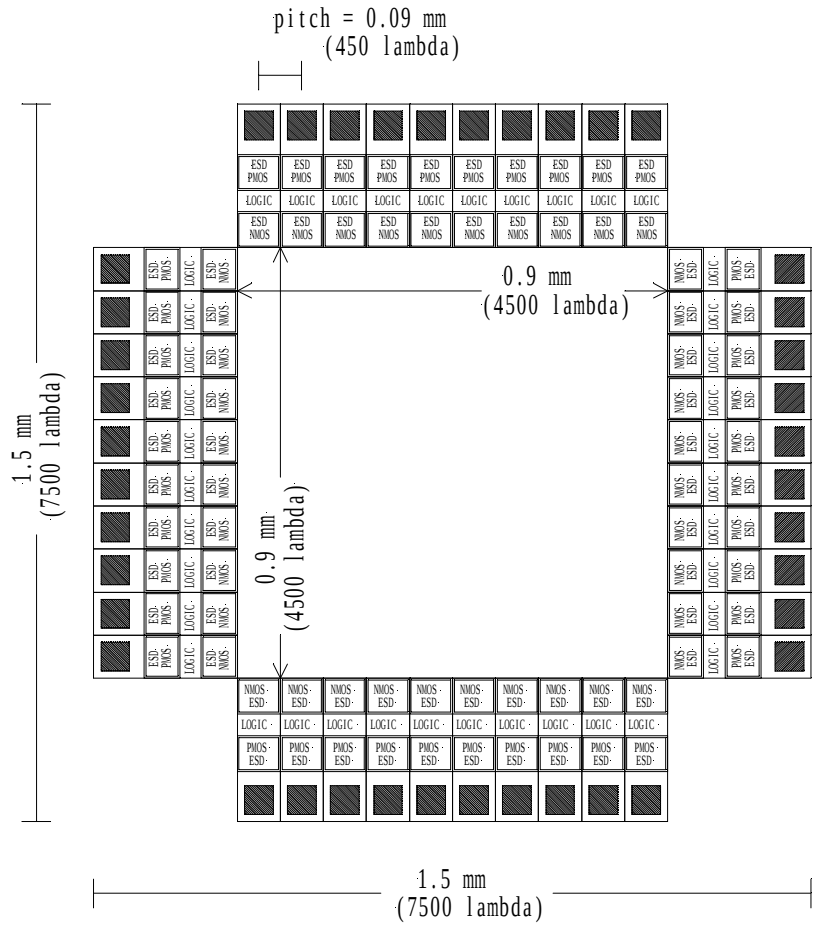
Protect Tanner Research's Engineering Resources

Through the entire Client Project cycle, starting from bid and proposal to the end of the Project, the Client will contact various engineering resources within Tanner Research. These resources may include Tanner Research's employees and its associates (subcontracting firms or individuals). The Client agrees not to recruit or hire any of these individuals or contract with any firms during the three years following Project completion.

☐☑

MOSIS TSMC/HP 0.35um
Hi-ESD Minimum Pad Frame

(1) lambda = 0.20um

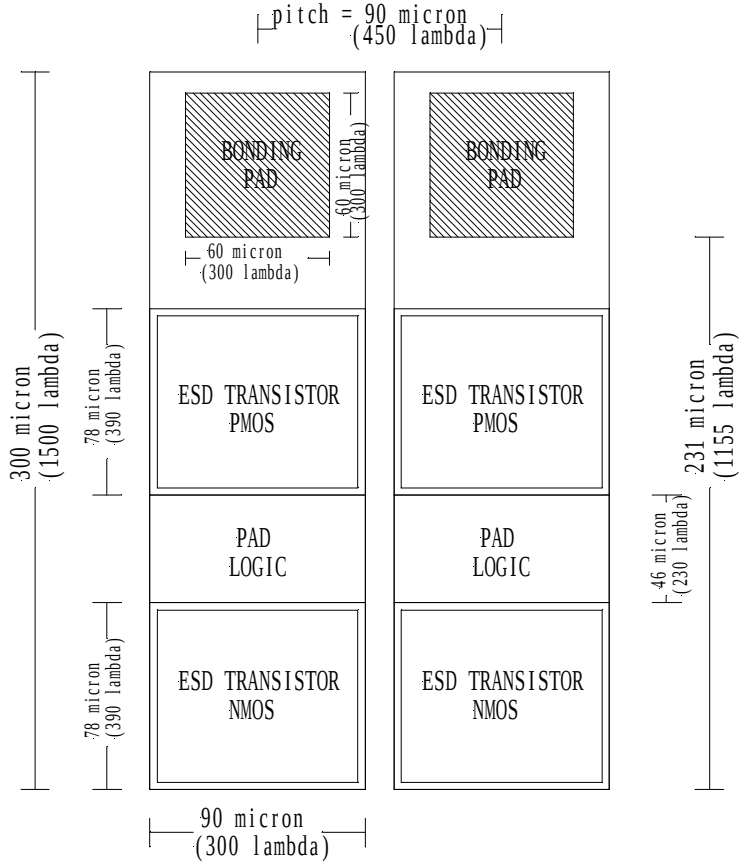


TANNER RESEARCH
2650 East Foothill Blvd, Pasadena, CA 91107
Tel: (626)792-3000
Fax: (626)792-0300

Created:Nov 9, 1998 15:15:18 Modified:Jun 15, 1999 13:36:11	Size: 5x7
Info:MOSIS TSMC/HP 0.35um Hi-ESD IO Pad Set	Rev A
Designer:Victor Dinh	
Module:Pad_Frame	Page:Page0
Path:O:\ces_prjct\mosis\Pad025-035U\work_dir\layout_TSMC035\mlou\databook\HiESD_Pad2	

MOSIS TSMC/HP 0.35um
Hi-ESD Pad Dimensions

(1) lambda = 0.20um



TANNER RESEARCH
2650 East Foothill Blvd, Pasadena, CA 91107
Tel: (626)792-3000
Fax: (626)792-0300

Created:Nov 9, 1998 13:20:00 Modified:Jun 15, 1999 13:34:21	Size: 5x7
Info:MOSIS TSMC/HP 0.35um Hi-ESD IO Pad Set	Rev A
Designer:Victor Dinh	
Module:Pad_Dimension	Page:Page0
Path:O:\ces_prjct\mosis\Pad025-035U\work_dir\layout_TSMC035\mlou\databook\HiESD_Pad2	

Description: Pad Library

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	Library
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	Lib_Pads
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
N/A	N/A	N/A	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

MOSIS TSMC 0.35um - Submicron Rules

Hi-ESD IO PAD SET

Input Pad with Buffer

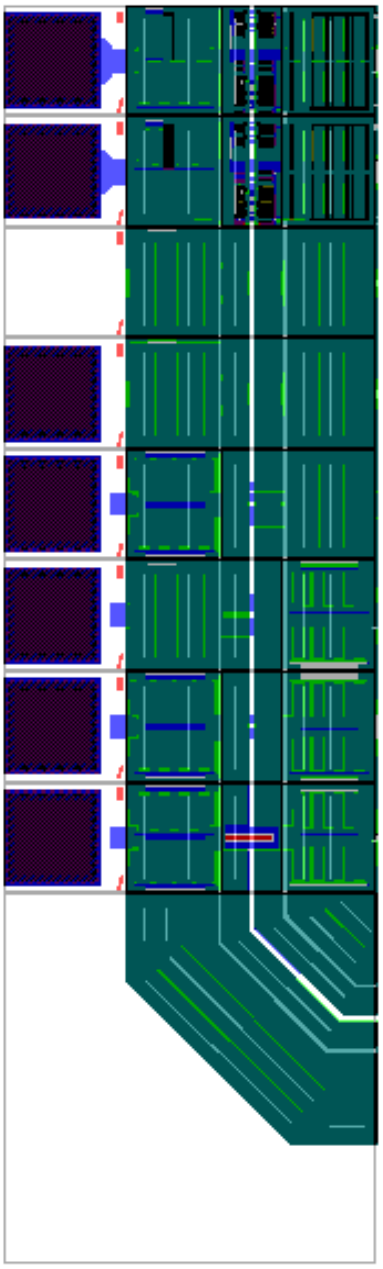
Vdd Pad with ESD

Gnd Pad with ESD

Analog Reference Pad with ESD

Analog IO Pad with ESD

Output Pad with Buffer



Description: Pad Frame

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	N/A
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035.tdb
	Cell:	FRAME
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

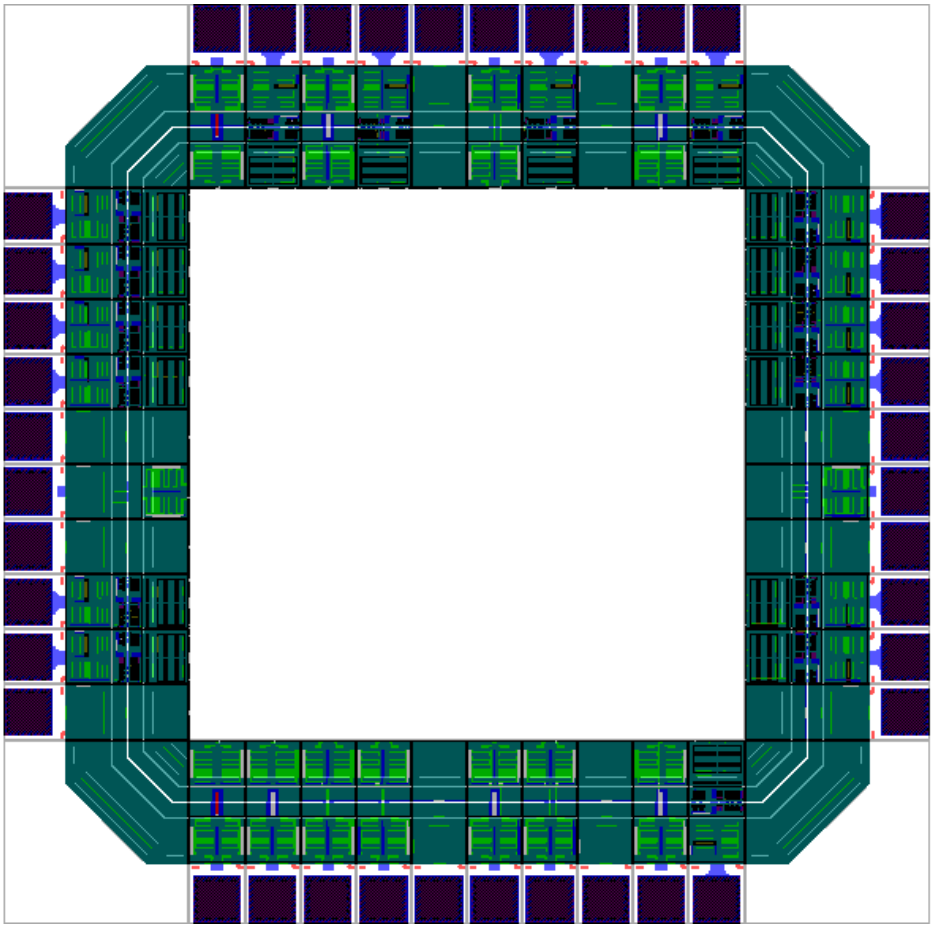
Height	Width	Area	Equivalent Gate	Drive
1.5 mm	1.5 mm	2.25 mm^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

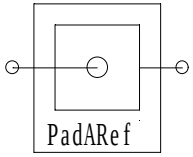
N/A



Analog Ref Pad PADAREF

Description: Analog Reference Pad

Library: MOSIS TSMC 035P
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\mTSMs035P.sdb
Module: PADAREF
Mask layout: L-Edit
File: TannerLb\scmos\mTSMs035P.tdb
Cell: PADAREF
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

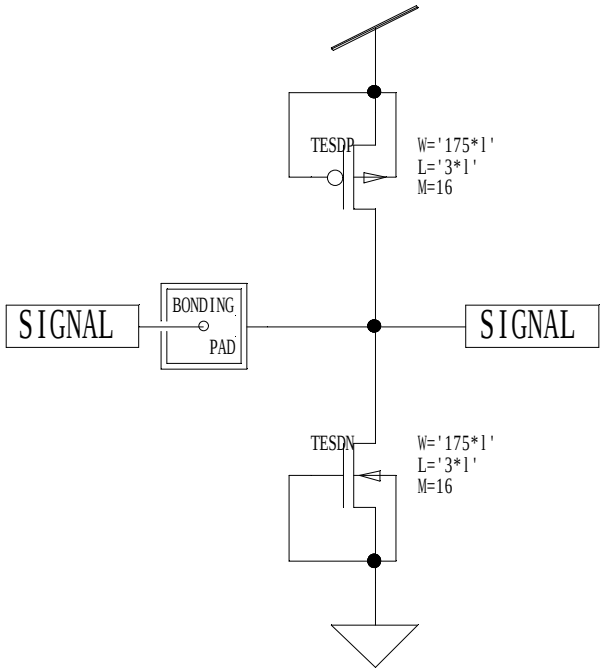
Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

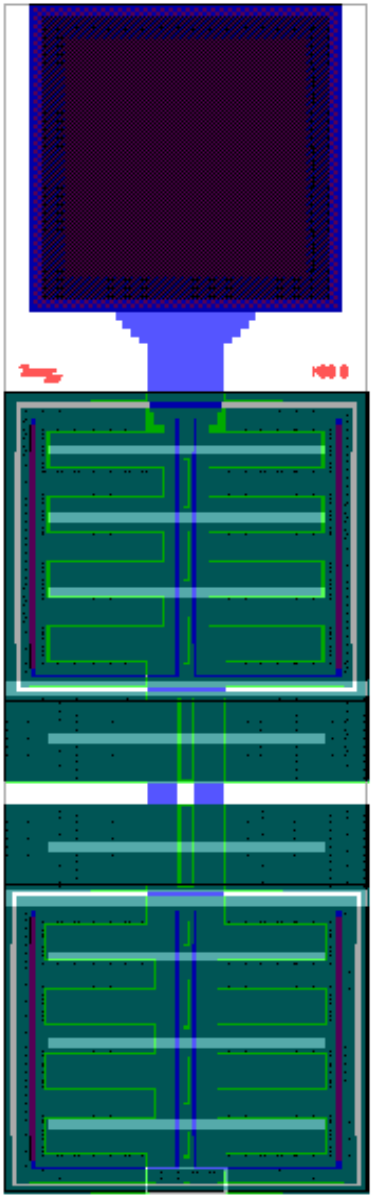
Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

PadARef

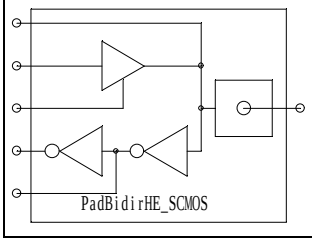




Bi-Directional Pad — PADBIDIR

Description: Bi-Directional Pad with Buffer

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	PADBIDIR
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	PADBIDIR
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

PAD	OE	DI	DO
X	1	X	In
1	0	1	X
0	0	0	X

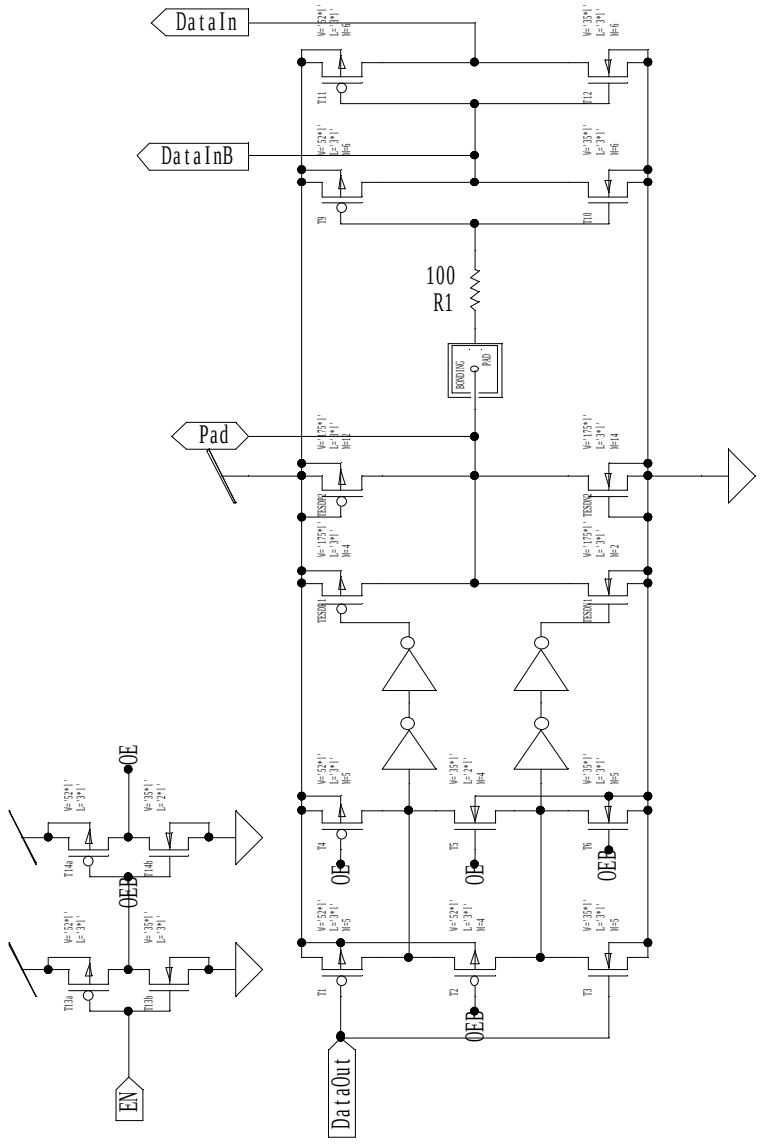
Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

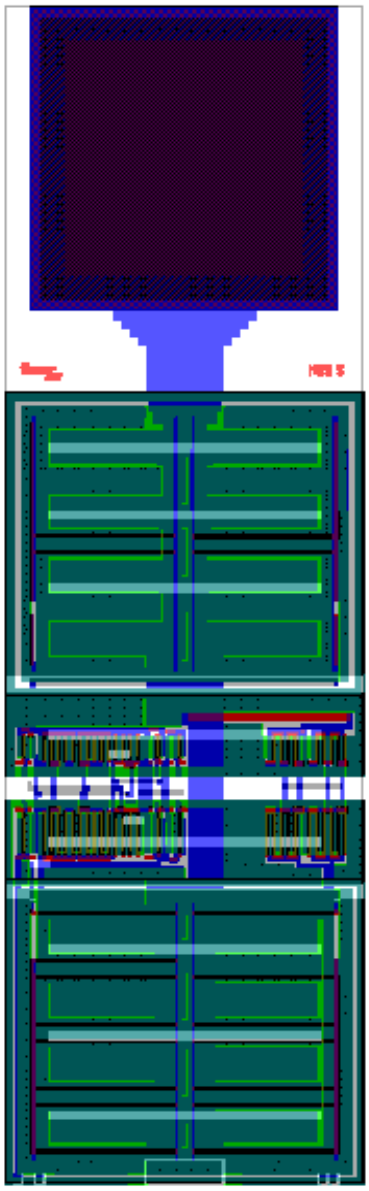
Logic Equation

See truth table

Delay Characteristics: N/A

This page is intentionally left blank.





Pad Frame Corner PADFC

Description: Pad Frame Corner

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	N/A
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	PADFC
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

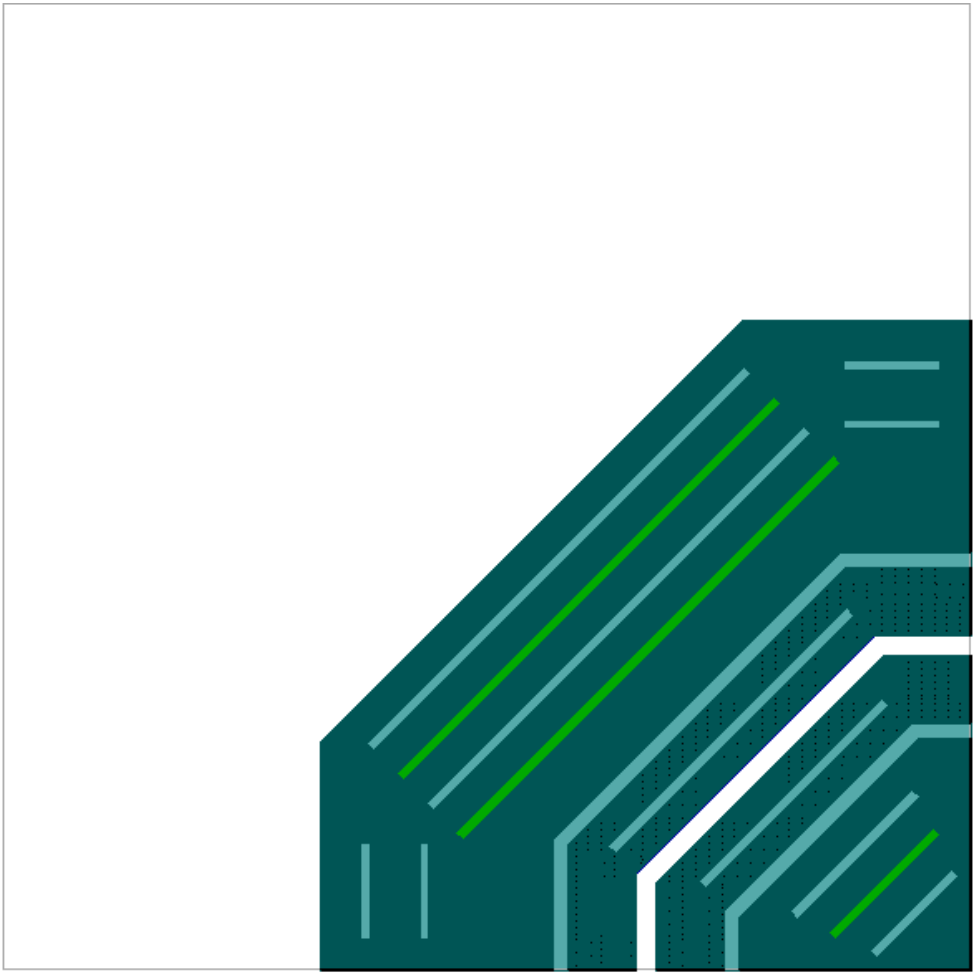
Height	Width	Area	Equivalent Gate	Drive
300 µ	300 µ	90000 μ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

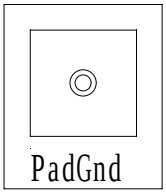
N/A



Ground Pad PADGND

Description: Ground Pad

Library: MOSIS TSMC 035P
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\mTSMs035P.sdb
Module: PADGND
Mask layout: L-Edit
File: TannerLb\scmos\mTSMs035P.tdb
Cell: PADGND
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

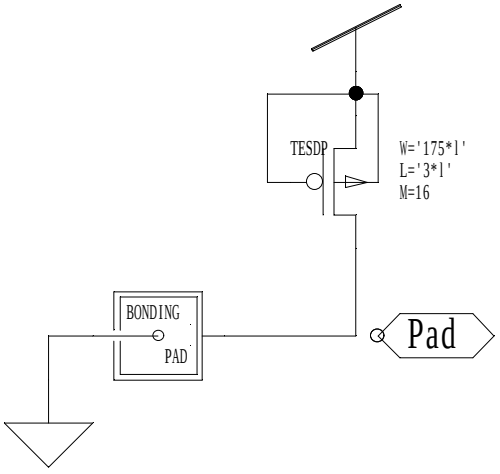
Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

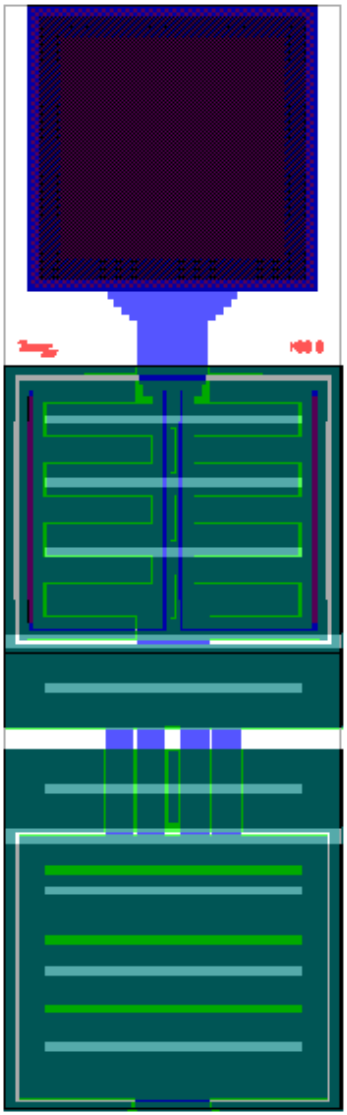
Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

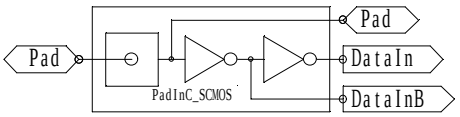
PadGnd





Description: Buffered Input Pad with Complementary Signals

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	PADINC
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	PADINC
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

PAD	DI	DIB
0	0	1
1	1	0

Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

Logic Equation

See truth table

Delay Characteristics:

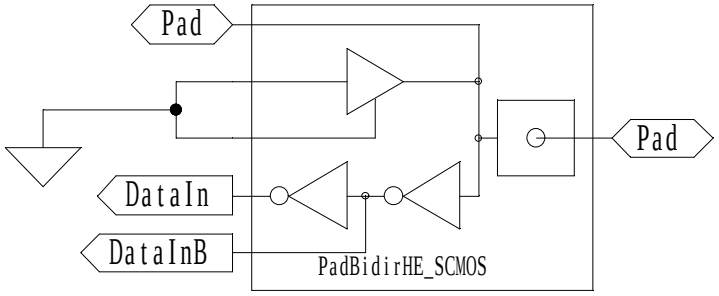
$T_{pd} = 0.28ns$

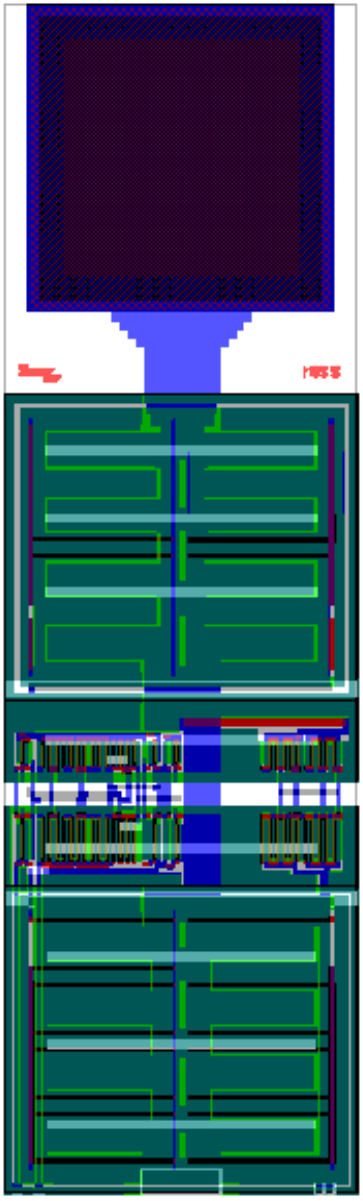
$T_r = 0.24ns$

$T_f = 0.18ns$

This page is intentionally left blank.

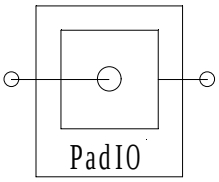
PadInC





Description: Input/Output Pad

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	PADIO
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	PADIO
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

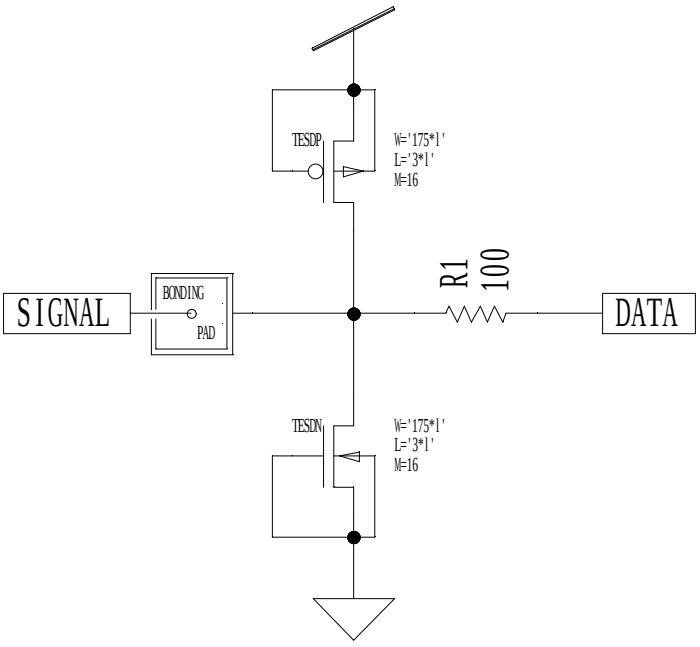
Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

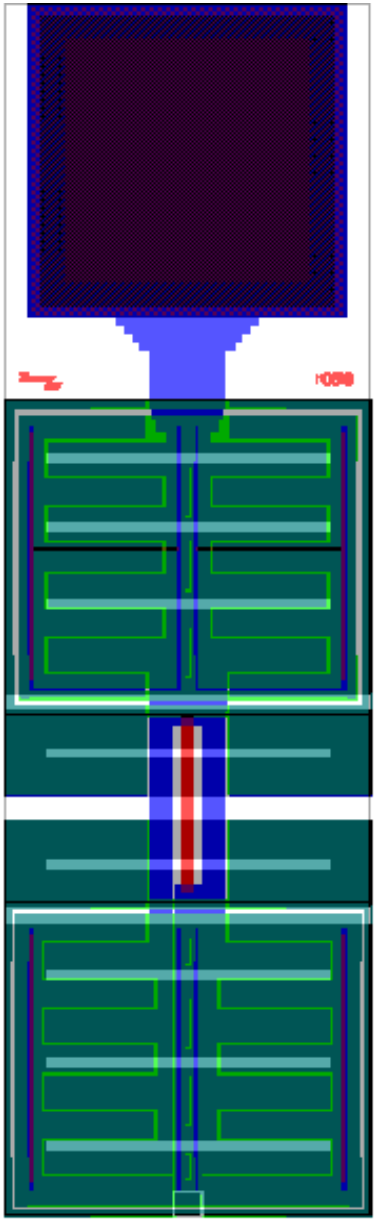
Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

PadIO





Padless Spacer PADSPACE

Description: Padless Spacer without Bonding Pad

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	N/A
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	PADSPACE
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

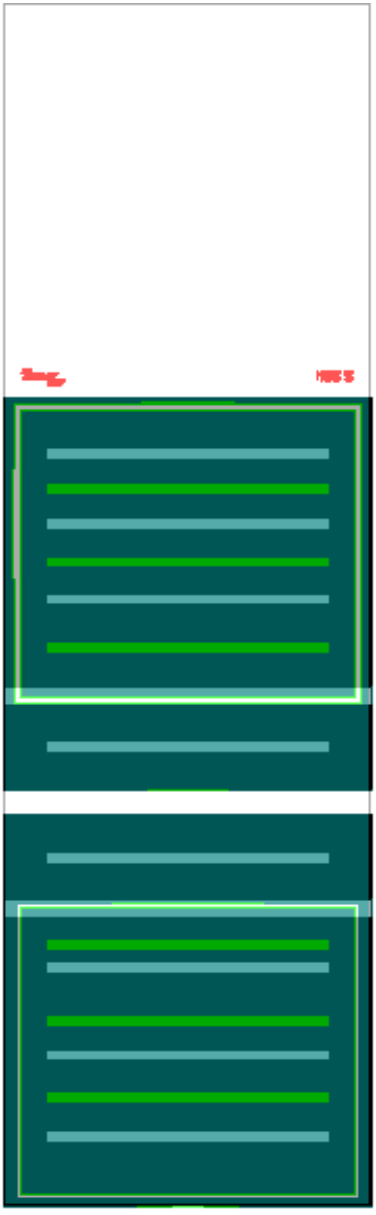
Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

N/A



Pad NoConnect PADNC

Description: Pad Spacer with No Connection to Bonding Pad

Library: MOSIS TSMC 035P
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\mTSMs035P.sdb
Module: N/A
Mask layout: L-Edit
File: TannerLb\scmos\mTSMs035P.tdb
Cell: PADNC
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

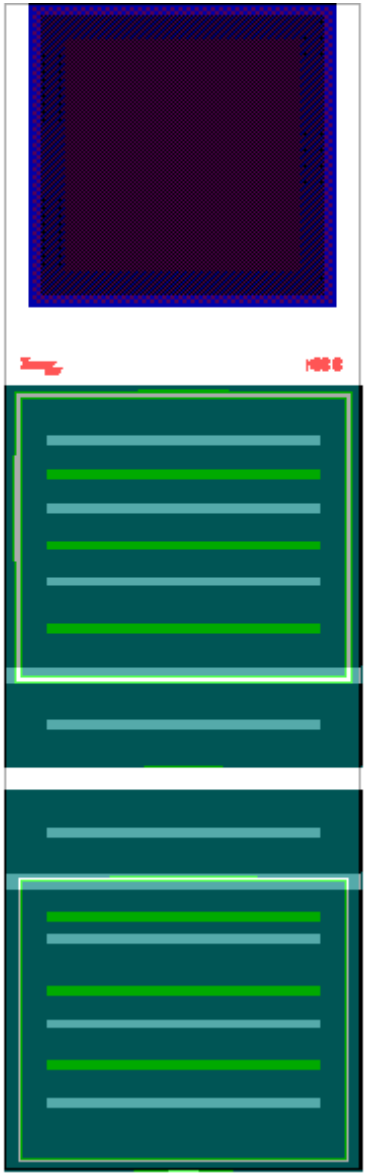
Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

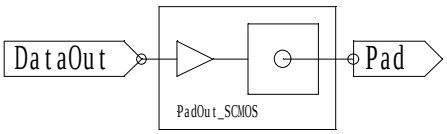
N/A



Output Pad — PADOUT

Description: Output Pad with Buffer

Library: MOSIS TSMC 035P	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\mTSMs035P.sdb
	Module:	PADOUT
Mask layout: L-Edit	File:	TannerLb\scmos\mTSMs035P.tdb
	Cell:	PADOUT
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	PAD | D0 0 | 0 1 | 1	N/A

Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

Logic Equation

$Pad = DataOut$

Delay Characteristics:

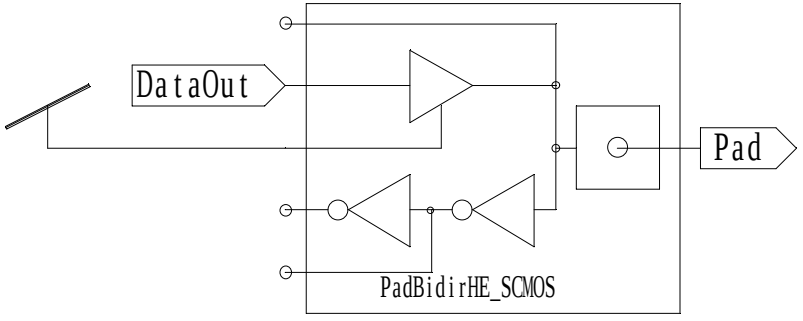
$T_{pd} = 1.92ns$

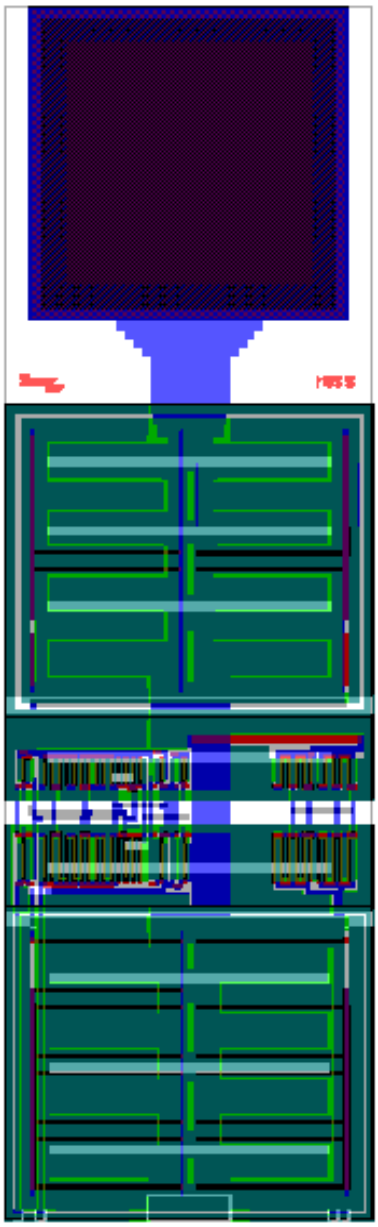
$T_r = 1.48ns$

$T_f = 1.23ns$

This page is intentionally left blank.

PadOut

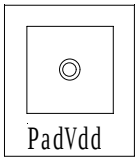




Power Pad PADVDD

Description: Power Pad

Library: MOSIS TSMC 035P
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\mTSMs035P.sdb
Module: PADVDD
Mask layout: L-Edit
File: TannerLb\scmos\mTSMs035P.tdb
Cell: PADVDD
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
300 µ	90 µ	27000 μ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

This page is intentionally left blank.

PadVdd