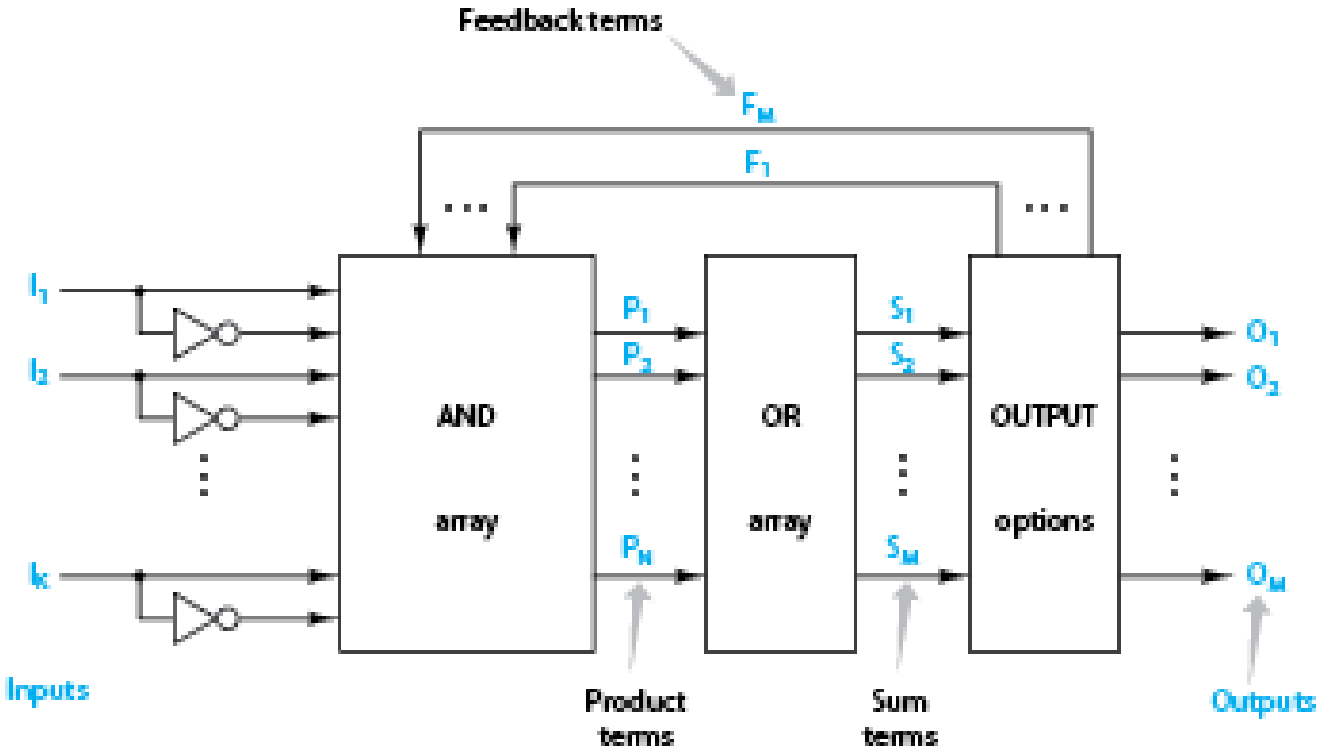
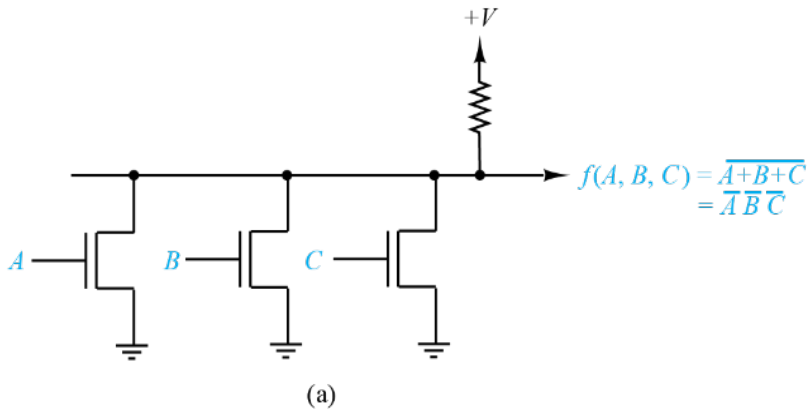
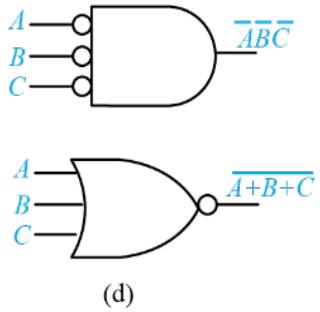
Programmable logic device architecture



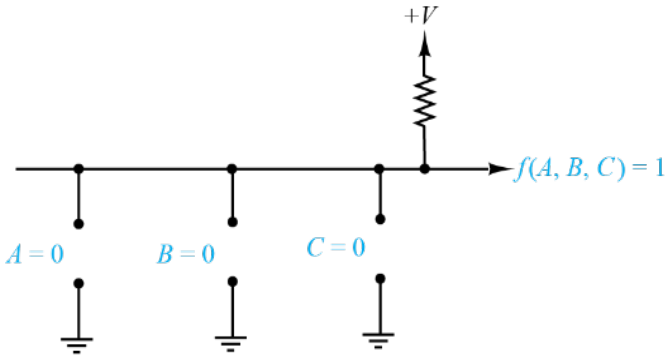
Transistors as switches in PLDs



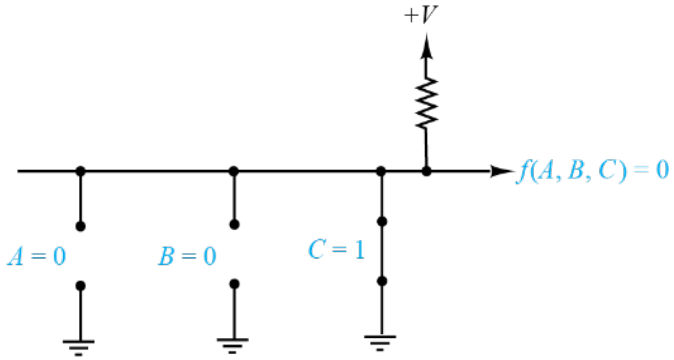
(a)



(d)



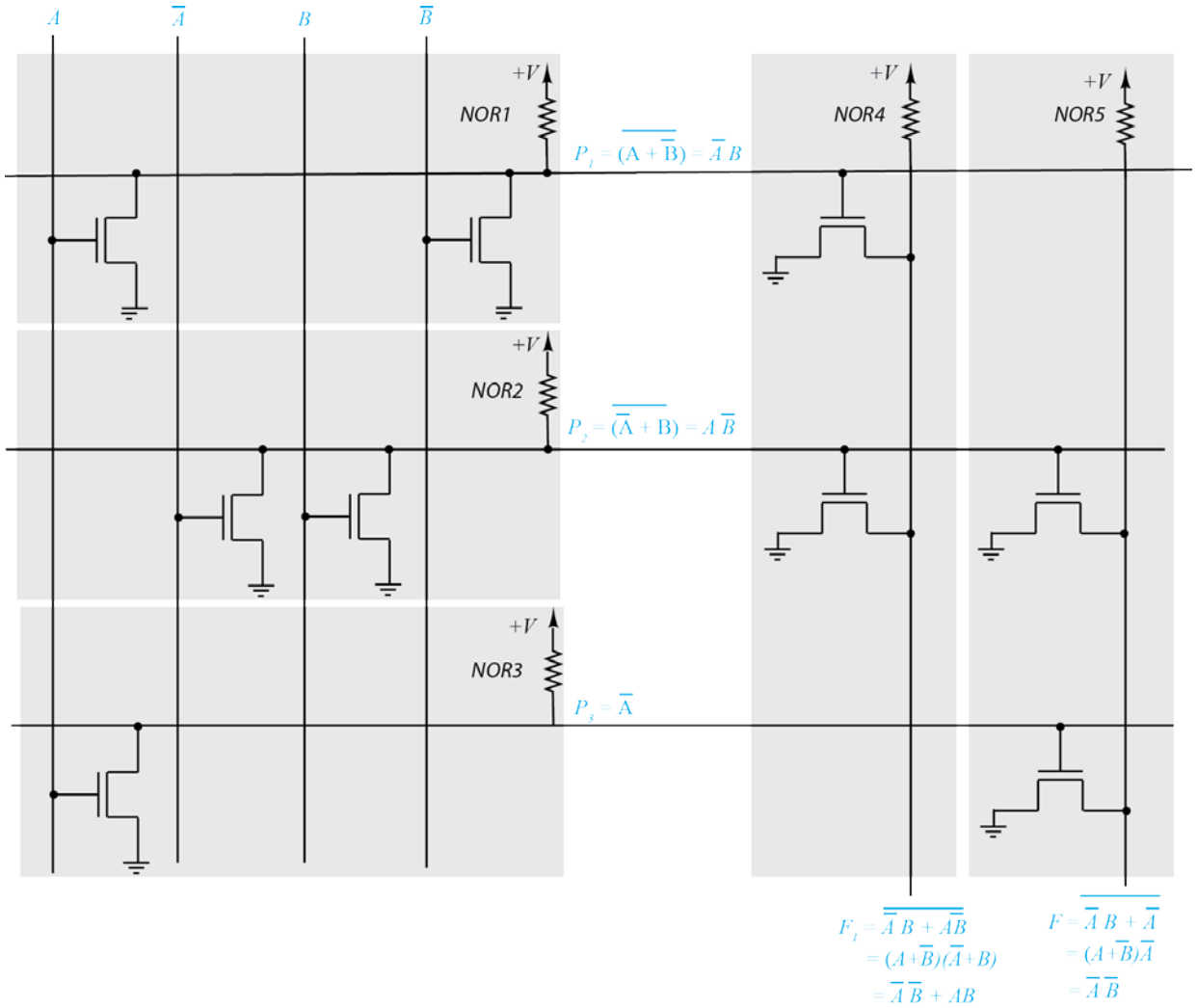
(b)

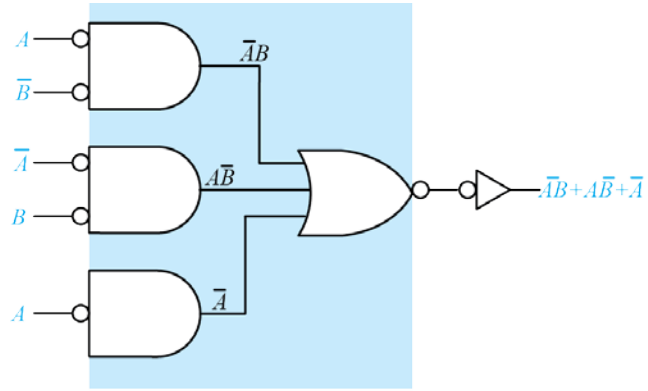


(c)

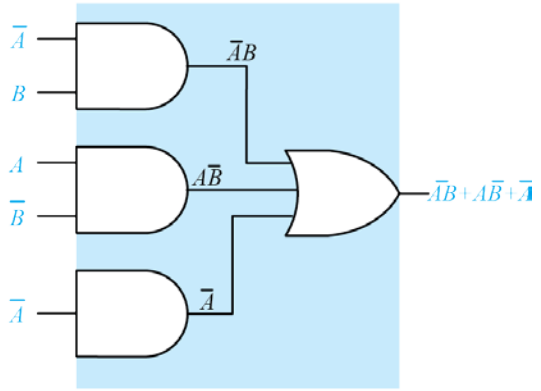
A B C	Q_A Q_B Q_C	F(A,B,C)
0 0 0	OFF OFF OFF	1
0 0 1	OFF OFF ON	0
0 1 0	OFF ON OFF	0
0 1 1	OFF ON ON	0
1 0 0	ON OFF OFF	0
1 0 1	ON OFF ON	0
1 1 0	ON ON OFF	0
1 1 1	ON ON ON	0

NOR-NOR logic array



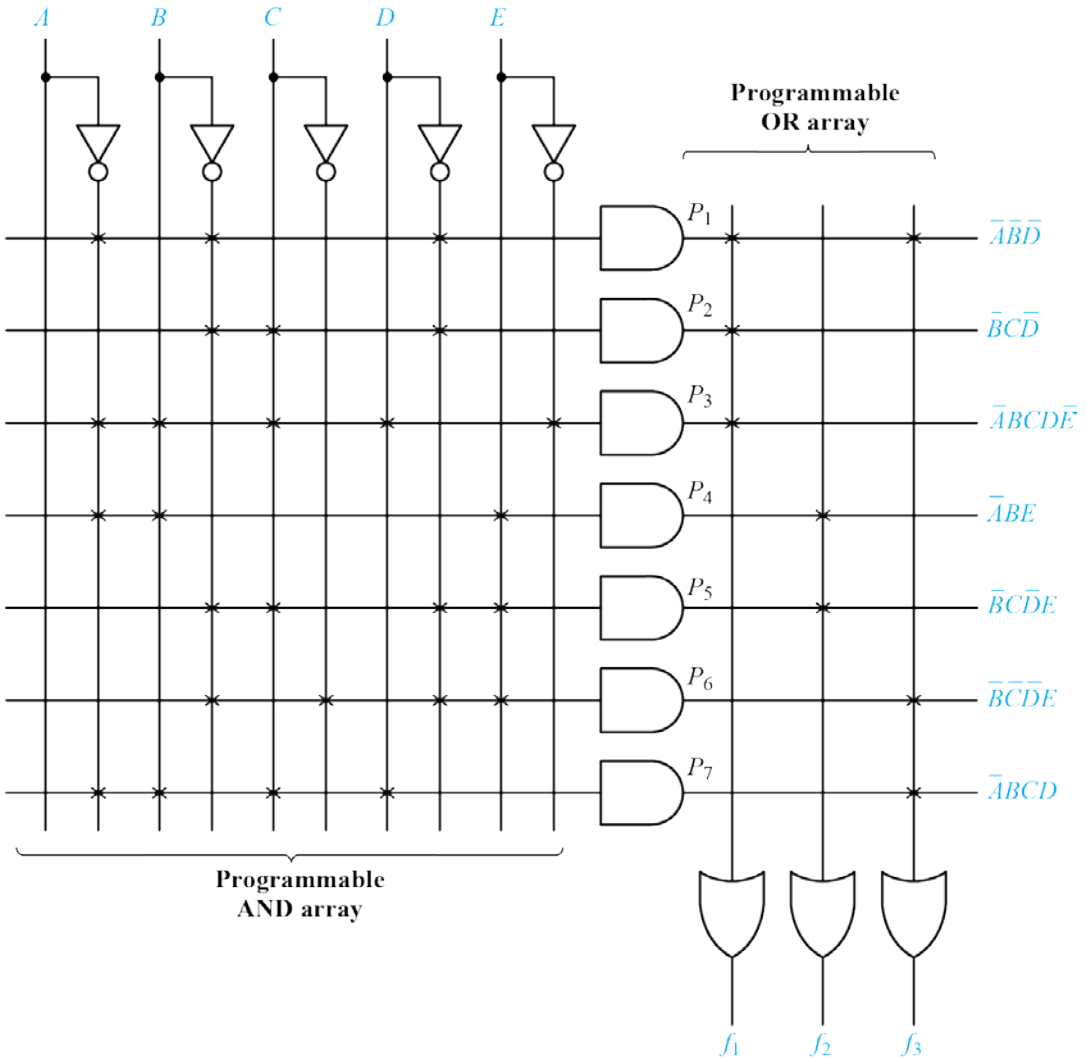


(a)



(b)

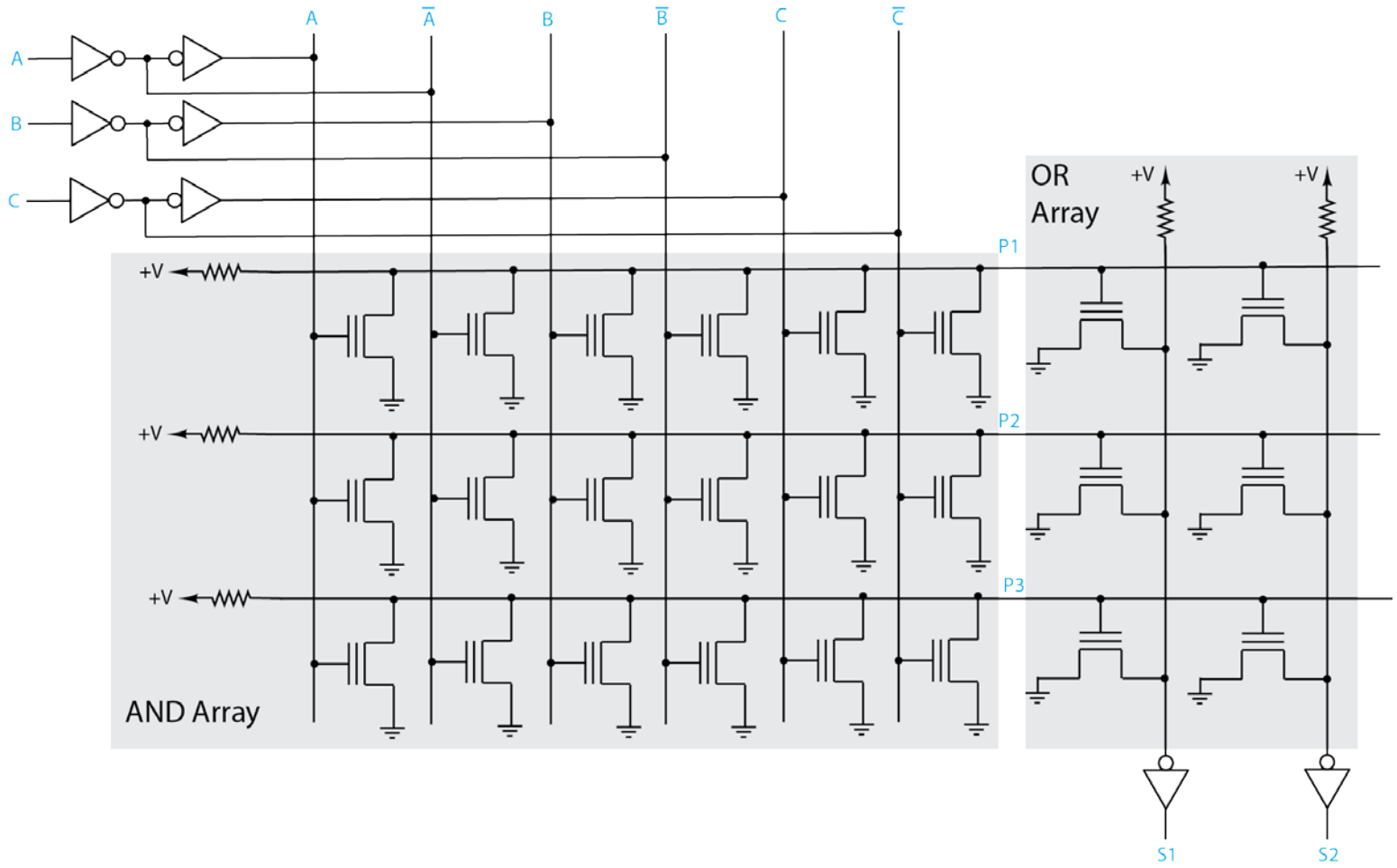
“Shorthand” representation of logic array



$$f_1(A,B,C,D,E) = \overline{A}\overline{B}\overline{D} + \overline{B}C\overline{D} + \overline{A}BCD\overline{E}$$
$$f_2(A,B,C,D,E) = \overline{A}BE + \overline{B}C\overline{D}E$$
$$f_3(A,B,C,D,E) = \overline{A}\overline{B}\overline{D} + \overline{B}\overline{C}\overline{D}E + \overline{A}BCD$$

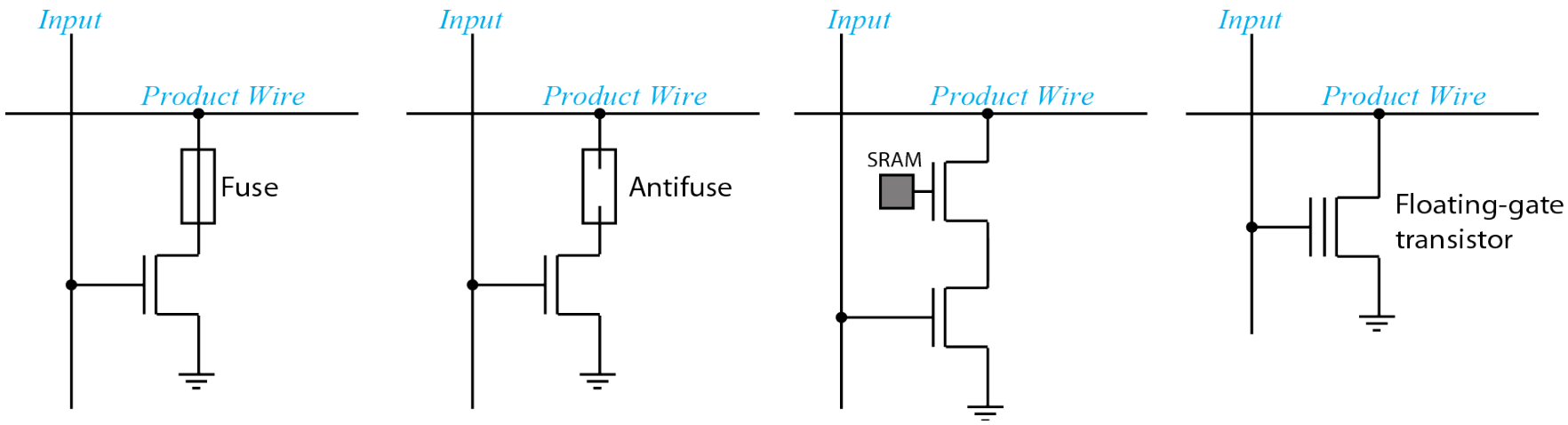
Product Term	Function(s)
$P1 = \overline{A} \cdot \overline{B} \cdot \overline{D}$	f_1, f_3
$P2 = \overline{B} \cdot C \cdot \overline{D}$	f_1
$P3 = \overline{A} \cdot B \cdot C \cdot D \cdot \overline{E}$	f_1
$P4 = \overline{A} \cdot B \cdot E$	f_2
$P5 = \overline{B} \cdot C \cdot \overline{D} \cdot E$	f_2
$P6 = \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot E$	f_3
$P7 = \overline{A} \cdot B \cdot C \cdot D$	f_3

Field-programmable logic array

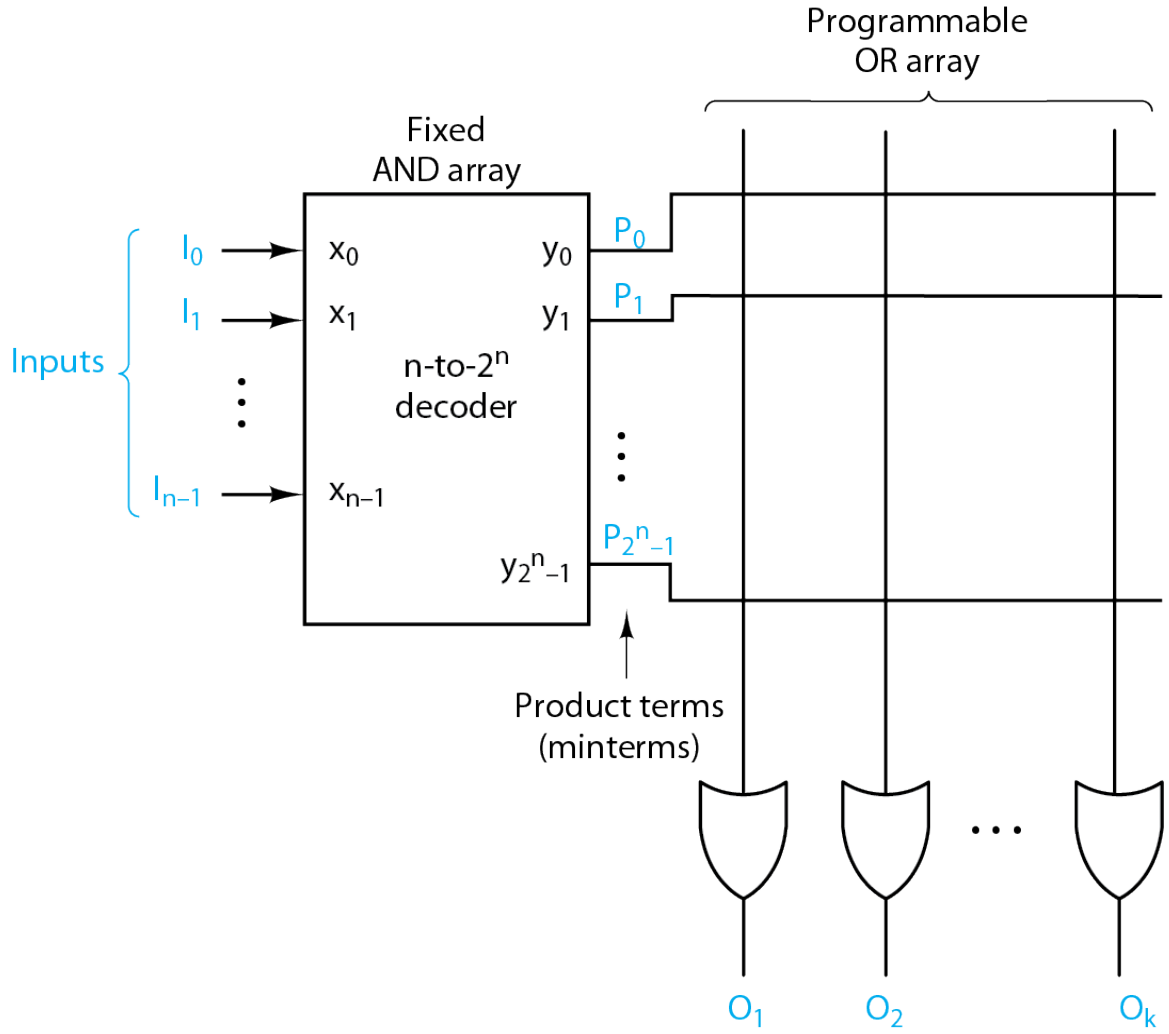


Floating-gate EEPROM transistors

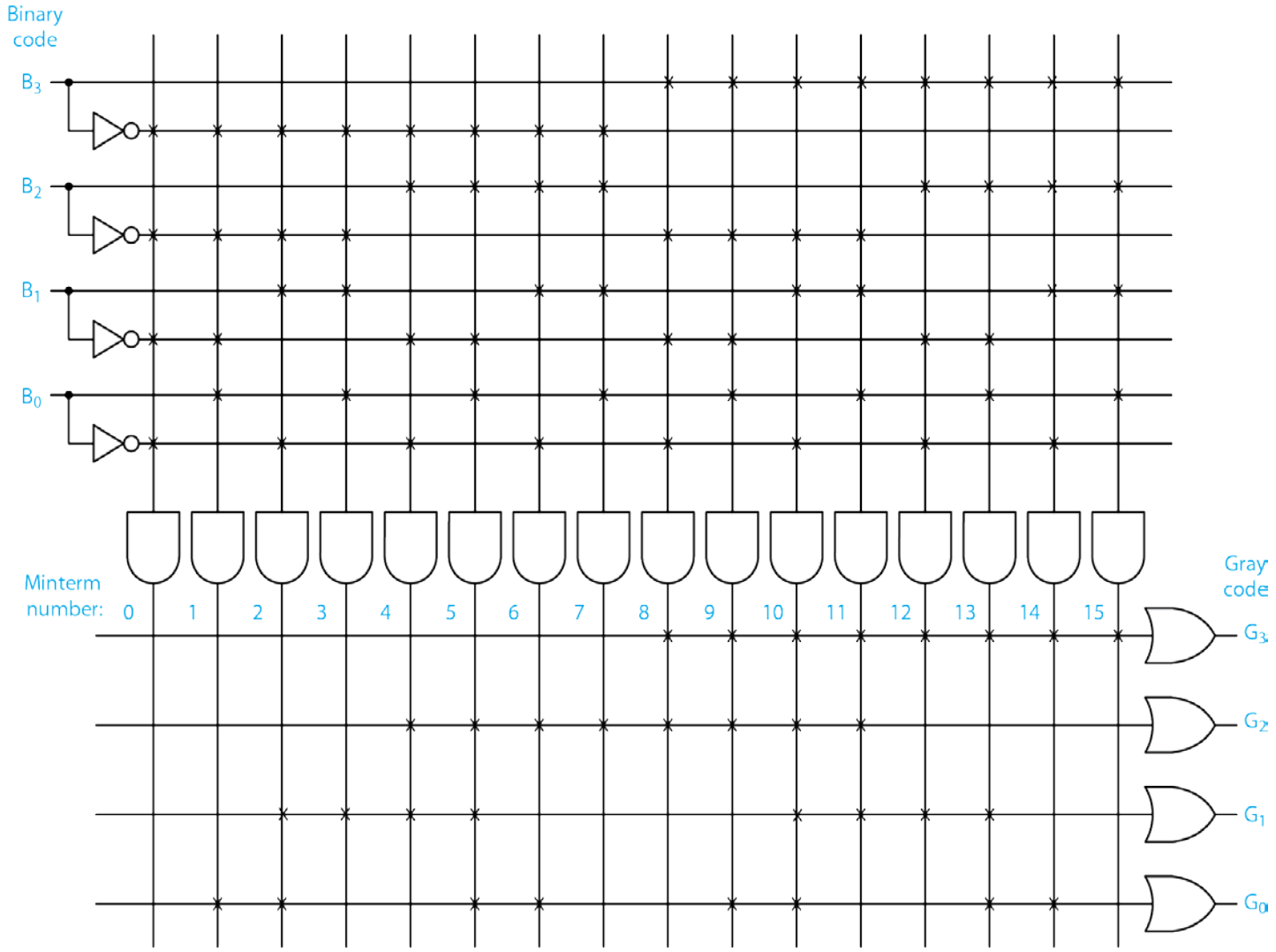
PLD programming technologies



PROM structure



Binary to gray code converter in PROM



Minterm Number	Binary $B_3B_2B_1B_0$	Gray Code $G_3G_2G_1G_0$
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

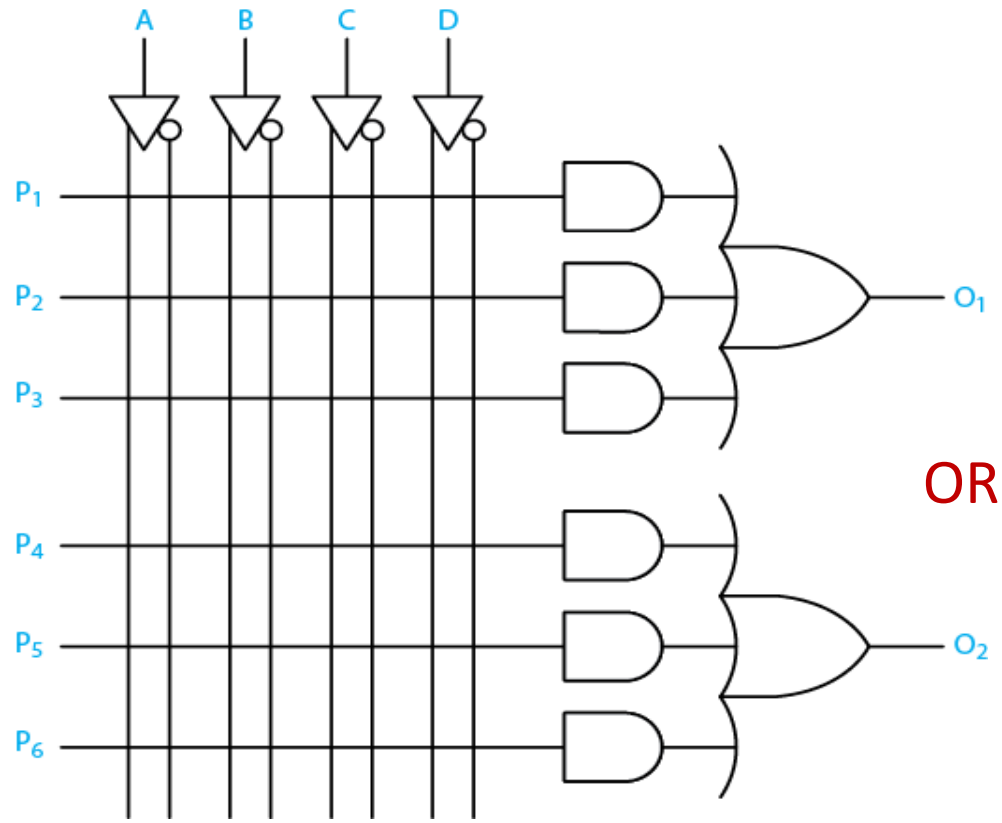
$$G_3 = \sum m(8,9,10,11,12,13,14,15)$$

$$G_2 = \sum m(4,5,6,7,8,9,10,11)$$

$$G_1 = \sum m(2,3,4,5,10,11,12,13)$$

$$G_0 = \sum m(1,2,5,6,9,10,13,14)$$

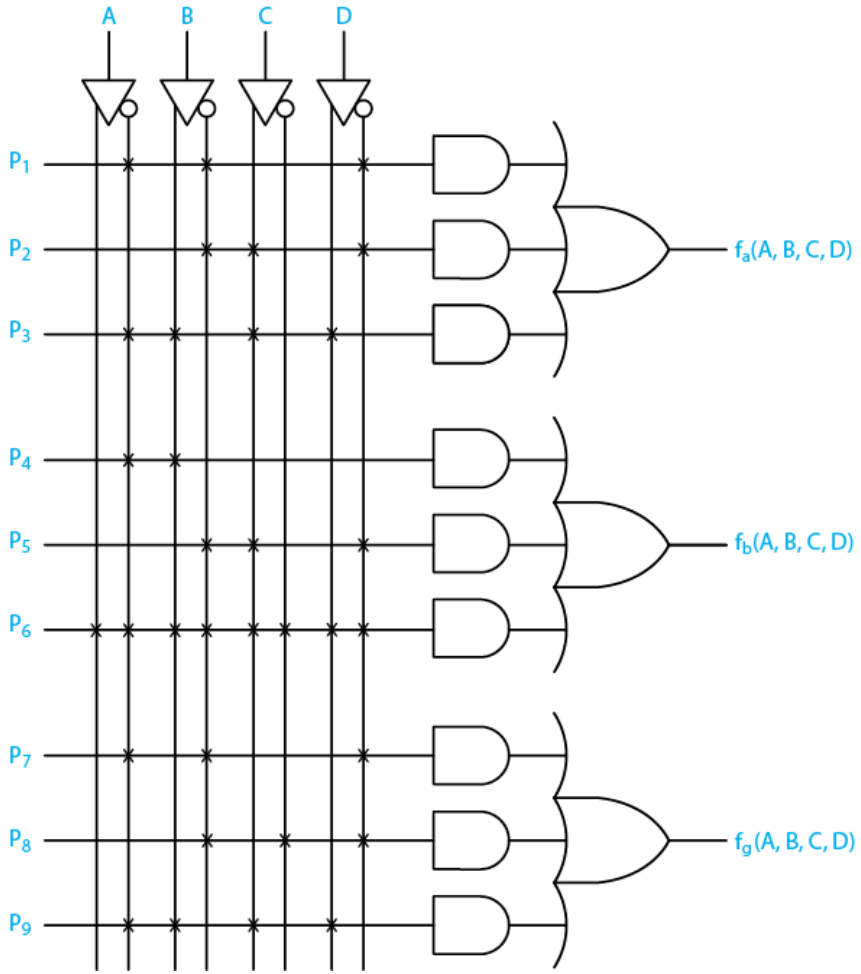
Programmable Array Logic (PAL)



OR array fixed

AND array programmable

PAL realization of function



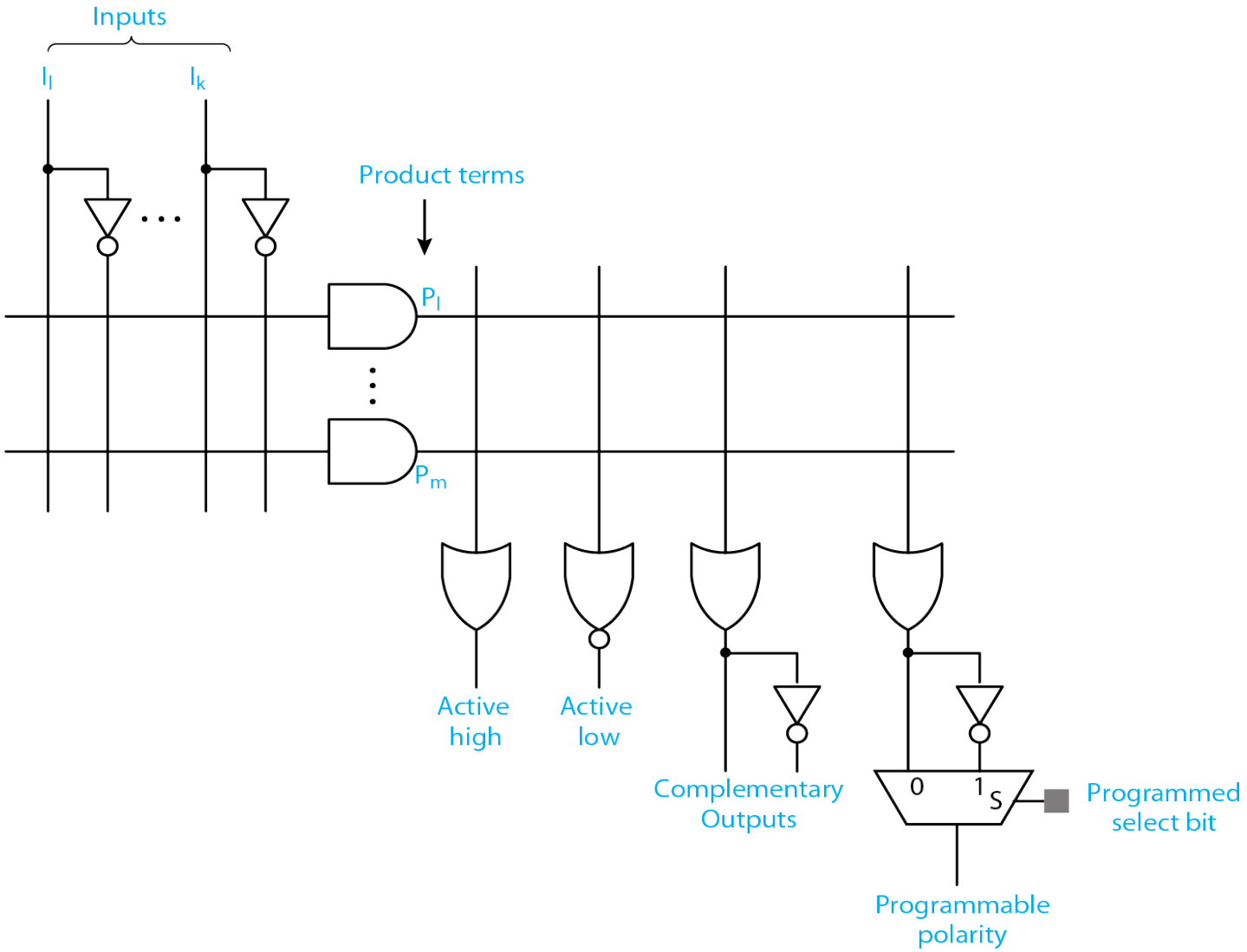
$$f_\alpha(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{D} + \overline{B}C\overline{D} + \overline{A}BCD$$

duplicated

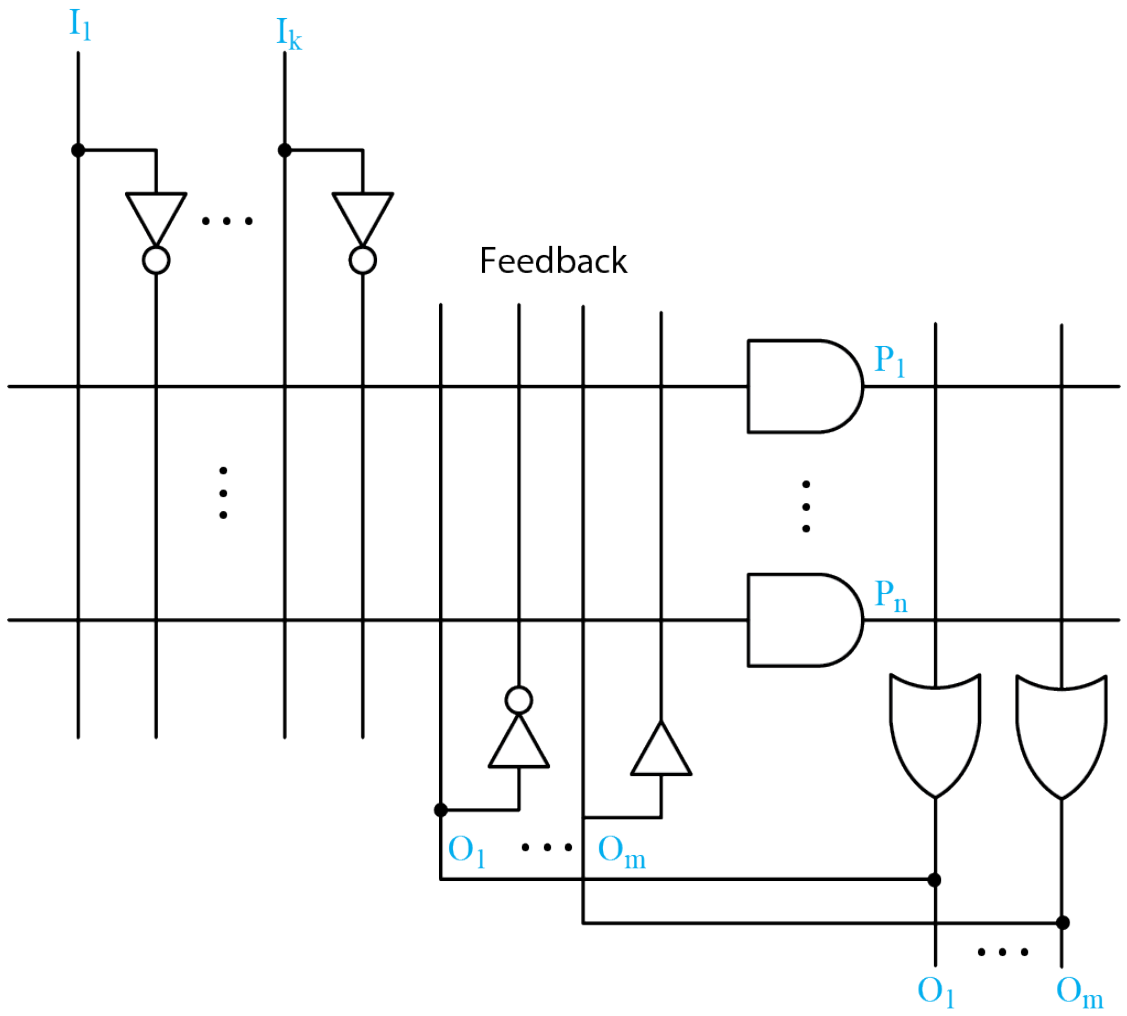
$$f_\beta(A,B,C,D) = \overline{A}B + \overline{B}C\overline{D}$$

$$f_\gamma(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{D} + \overline{B}\,\overline{C}\,\overline{D} + \overline{A}BCD$$

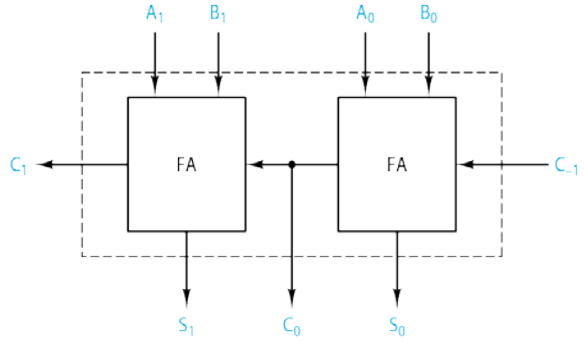
PLD output polarity options



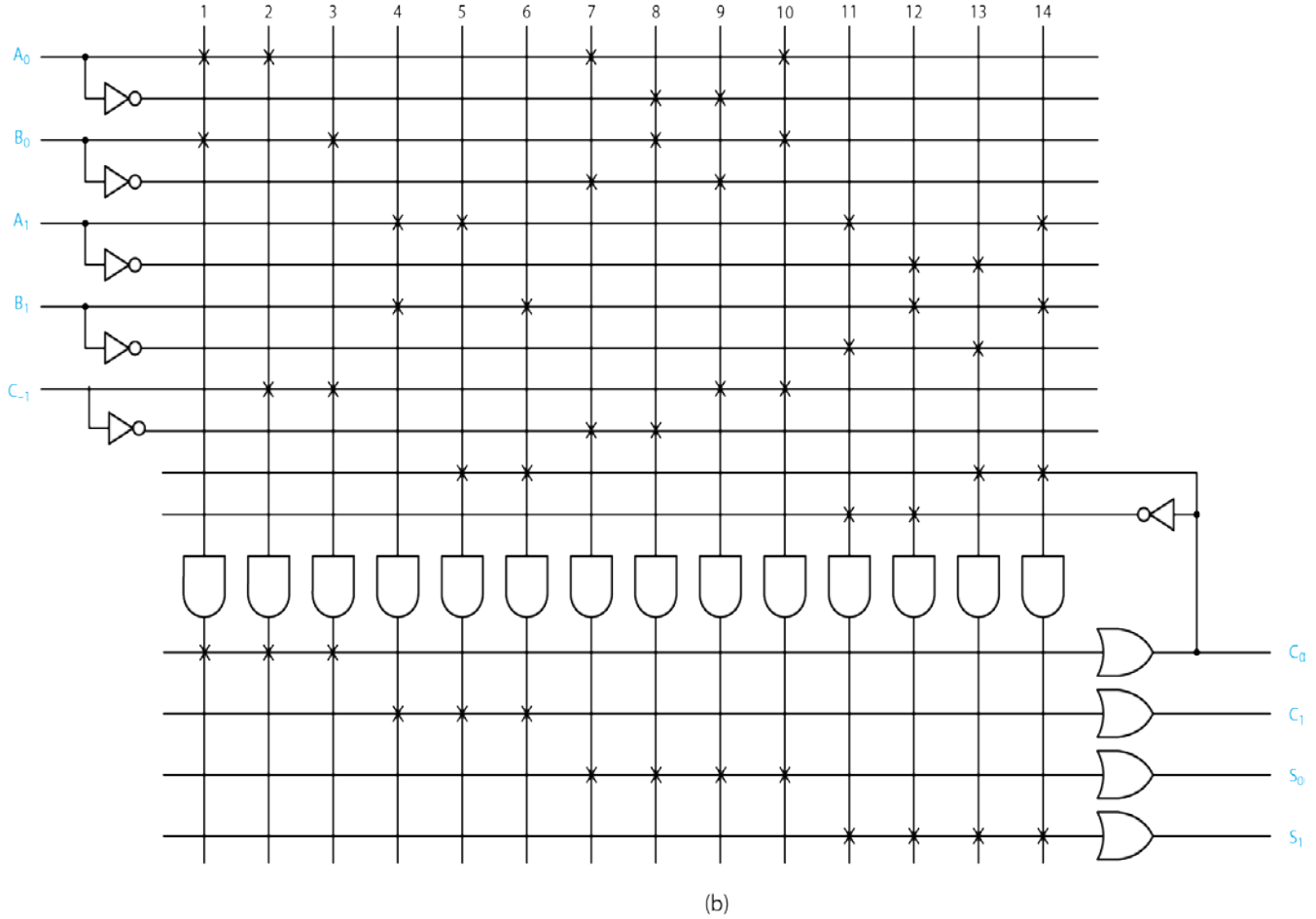
PLD output feedback



2-bit ripple-carry adder

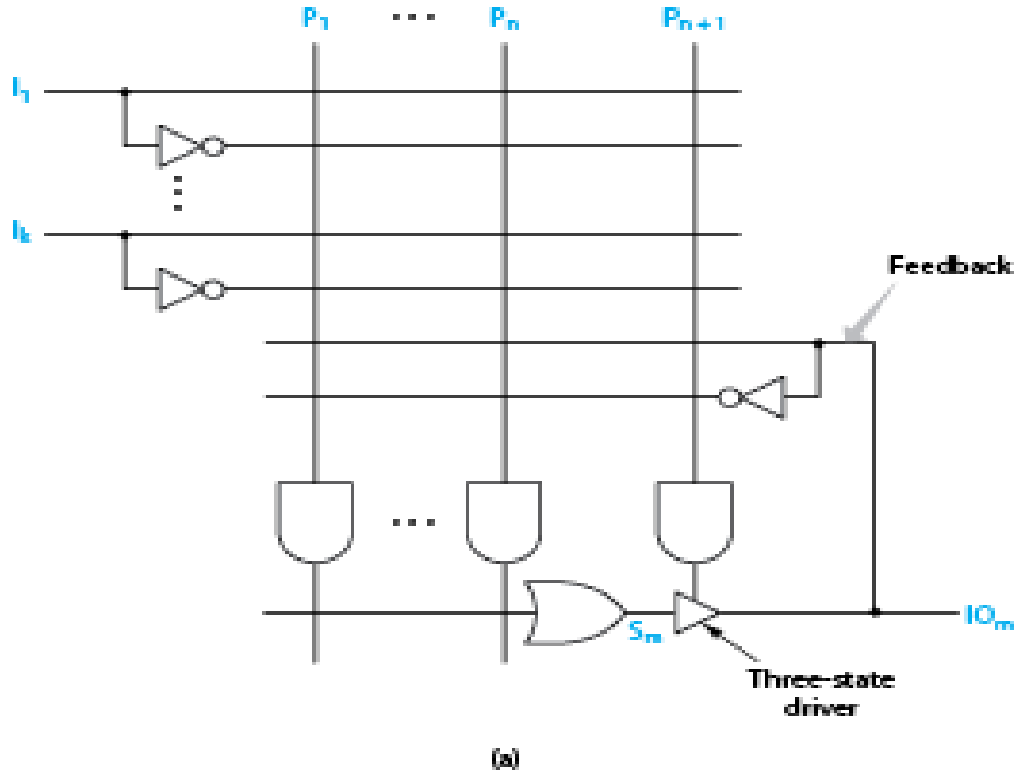


(a)

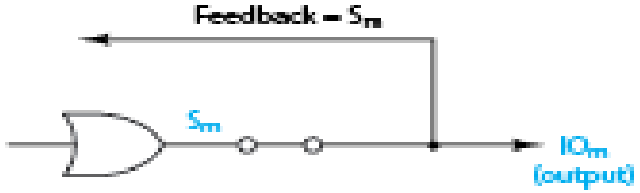


(b)

PLD bidirectional pins



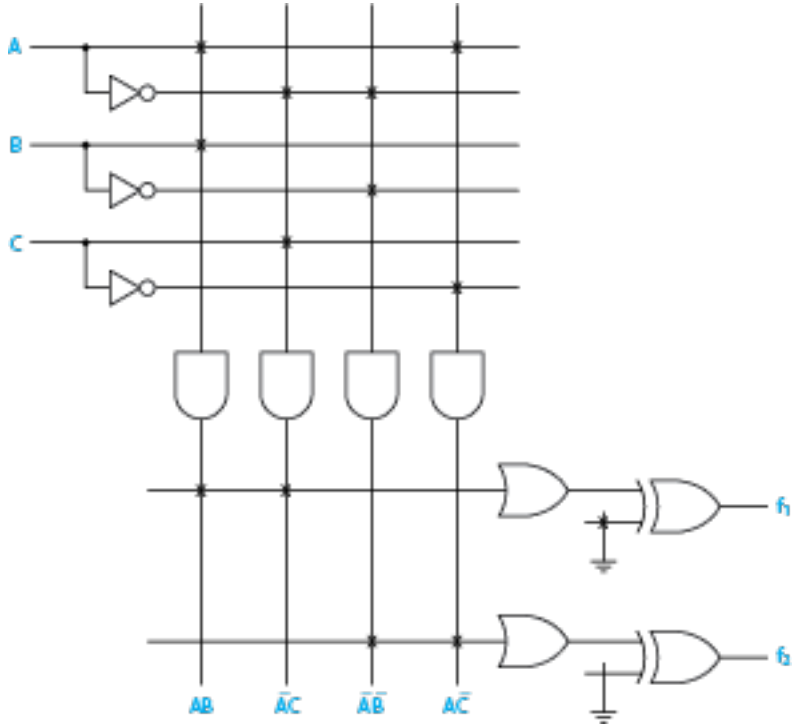
(a)



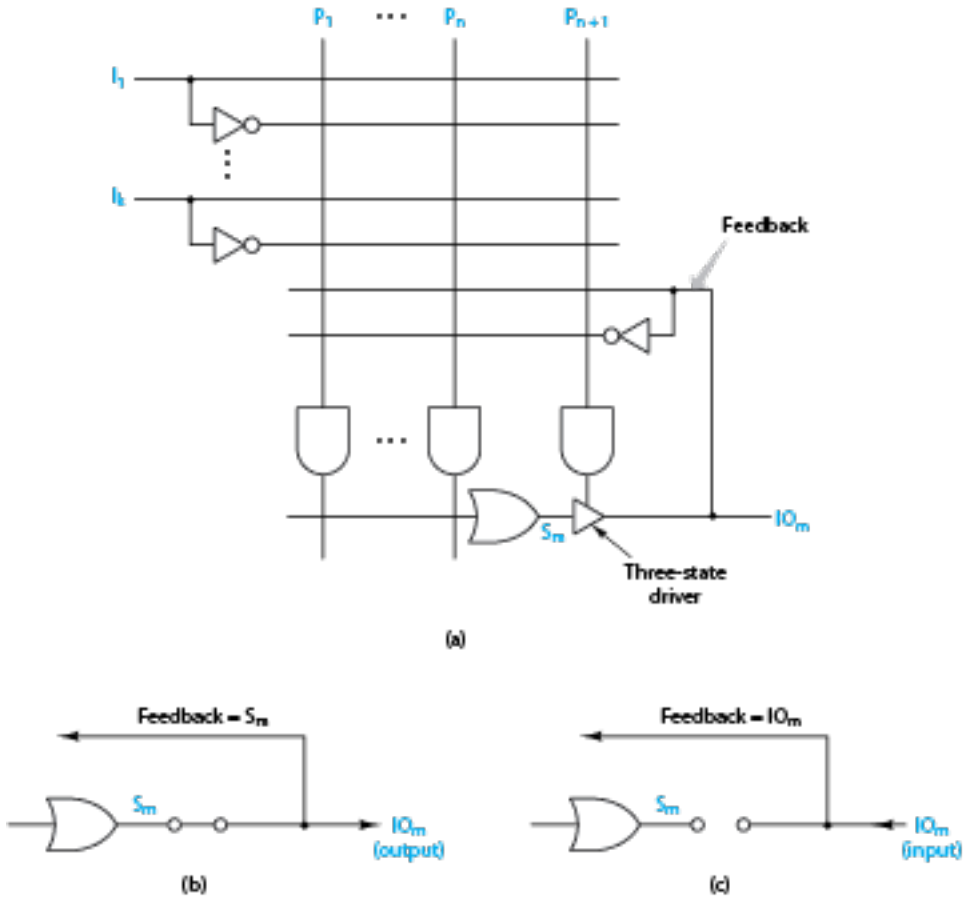
(b)

(c)

PLD output options

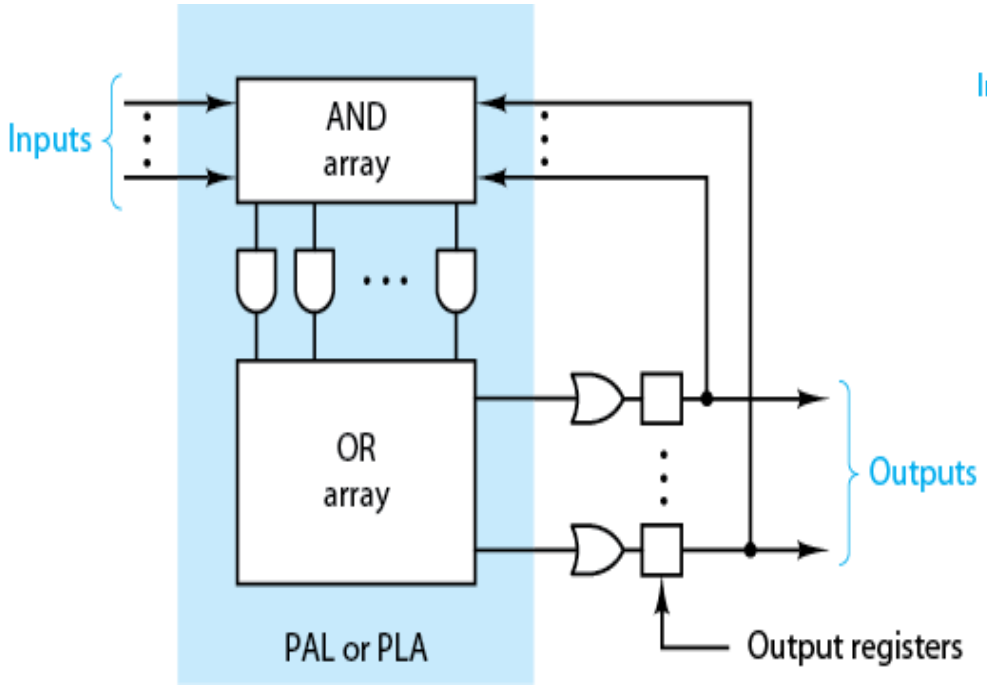


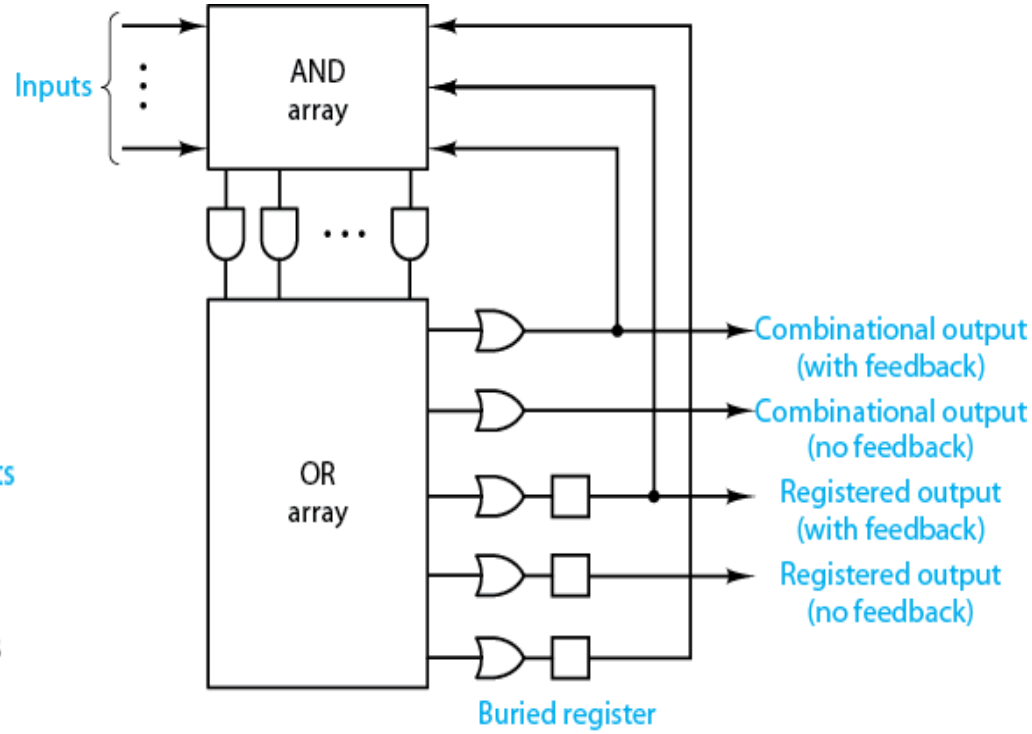
Programmable output polarity



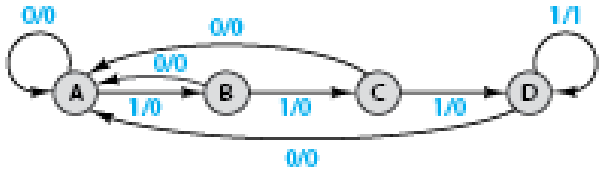
Output fed back to AND array

Registered outputs





FSM – sequence 1111 recognizer



(a)

	x = 0	x = 1
A	A/0	B/0
B	A/0	C/0
C	A/0	D/1
D	A/0	D/0

$y_1^k y_2^k$	x = 0	x = 1
00	00	01
01	00	10
11	00	11
10	00	11

$y_1^{k+1} y_2^{k+1}$

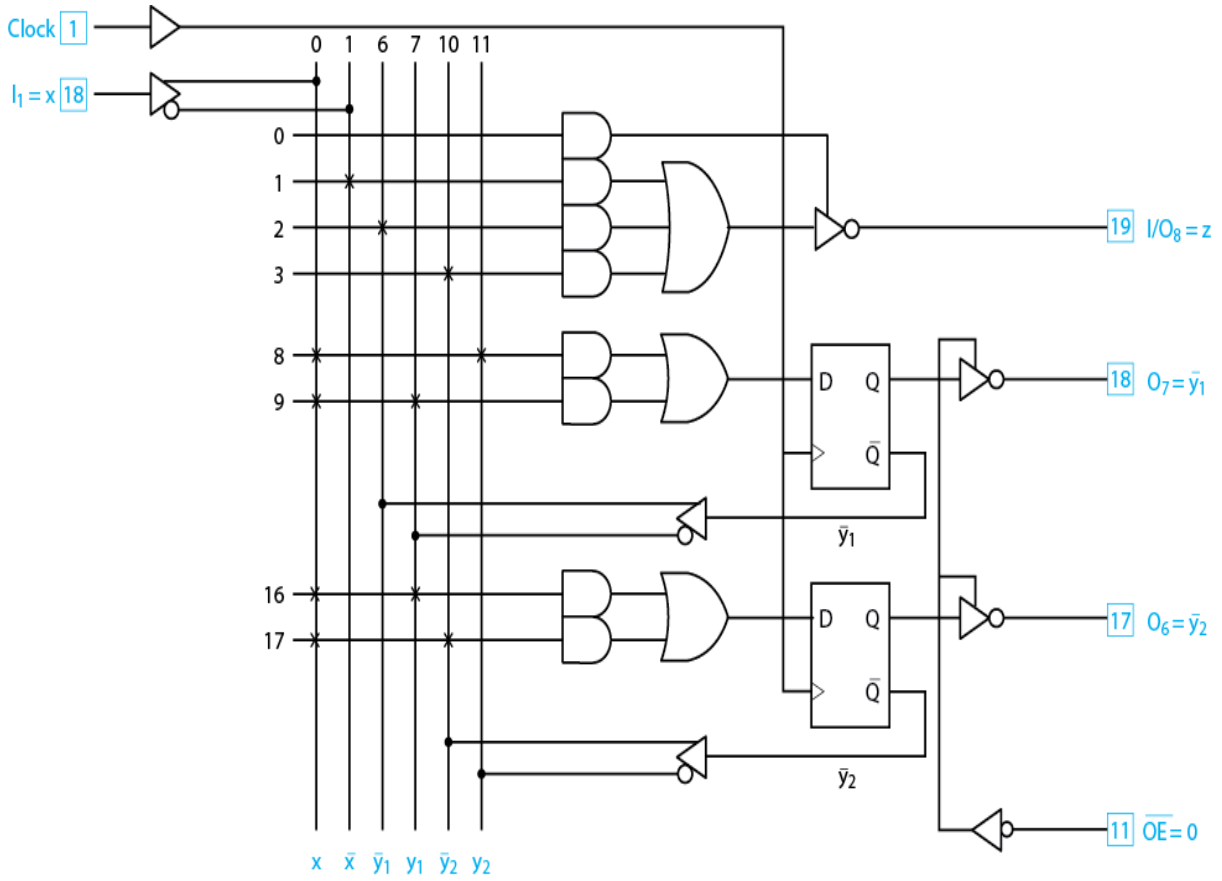
$y_1^k y_2^k$	x = 0	x = 1
00	0	0
01	0	0
11	0	1
10	0	0

z

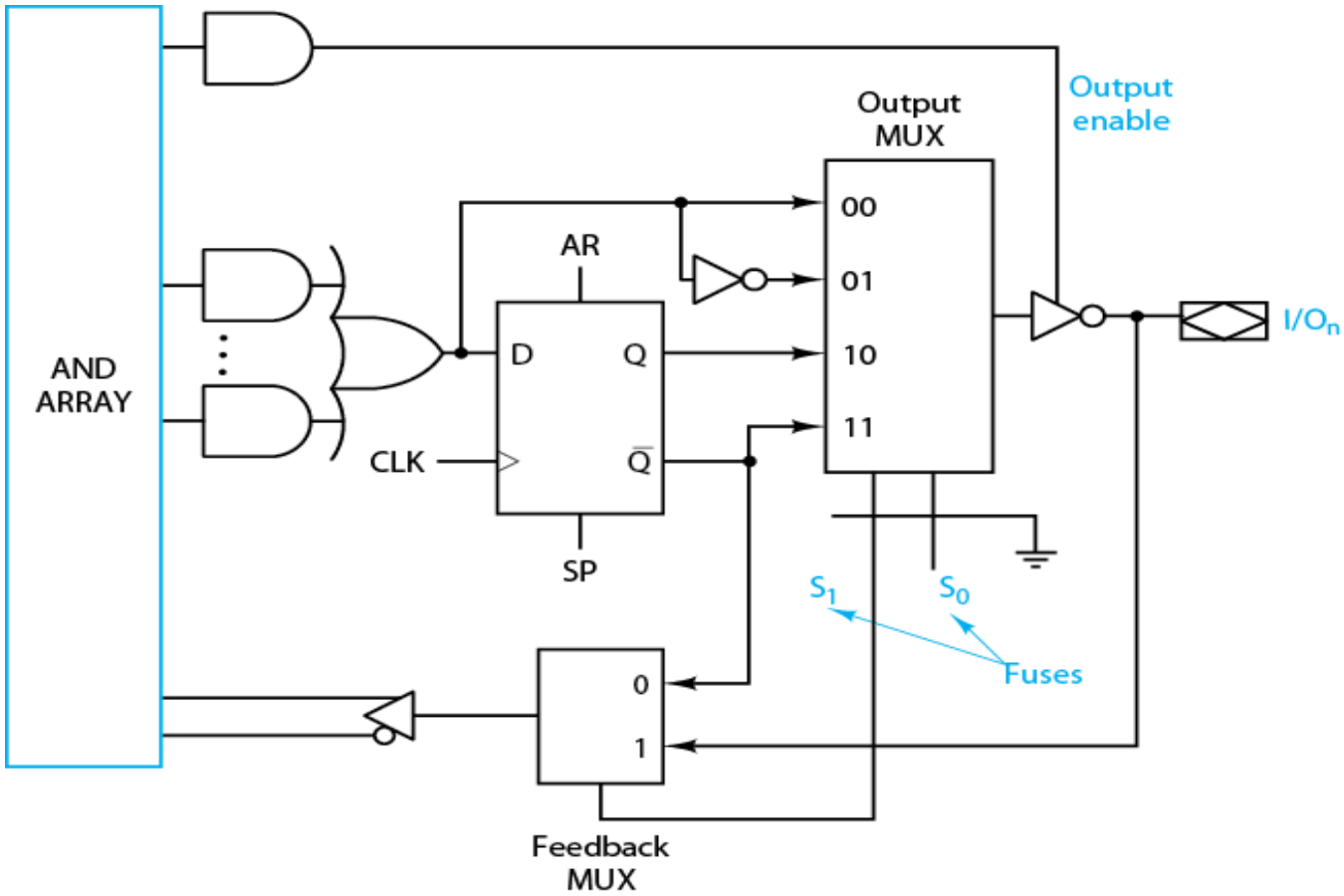
$$D_1 = xy_1 + xy_2$$

$$D_2 = xy_1 + x\bar{y}_2$$

$$z = xy_1y_2 = \overline{\bar{x} + \bar{y}_1 + \bar{y}_2}$$



PAL output “macrocell”



PAL22V10 PLD

- 44x132 PAL
- 10 macrocells
- 44 inputs
- 12 outputs
- 10 feedbacks