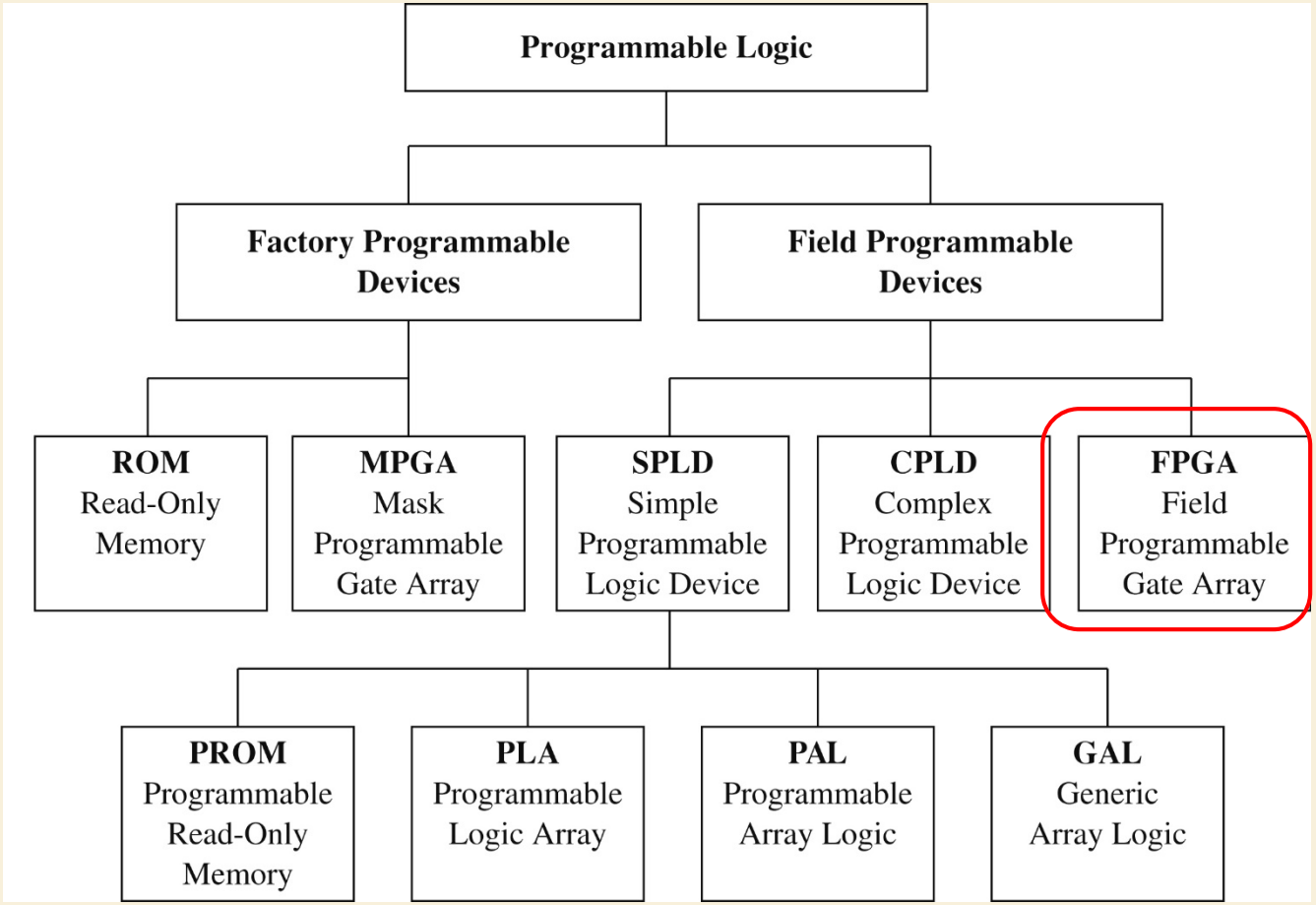
FIELD PROGRAMMABLE GATE ARRAYS (FPGAS)

Roth Text: Chapter 3 (section 3.4)

Chapter 6

Nelson Text: Chapter 11

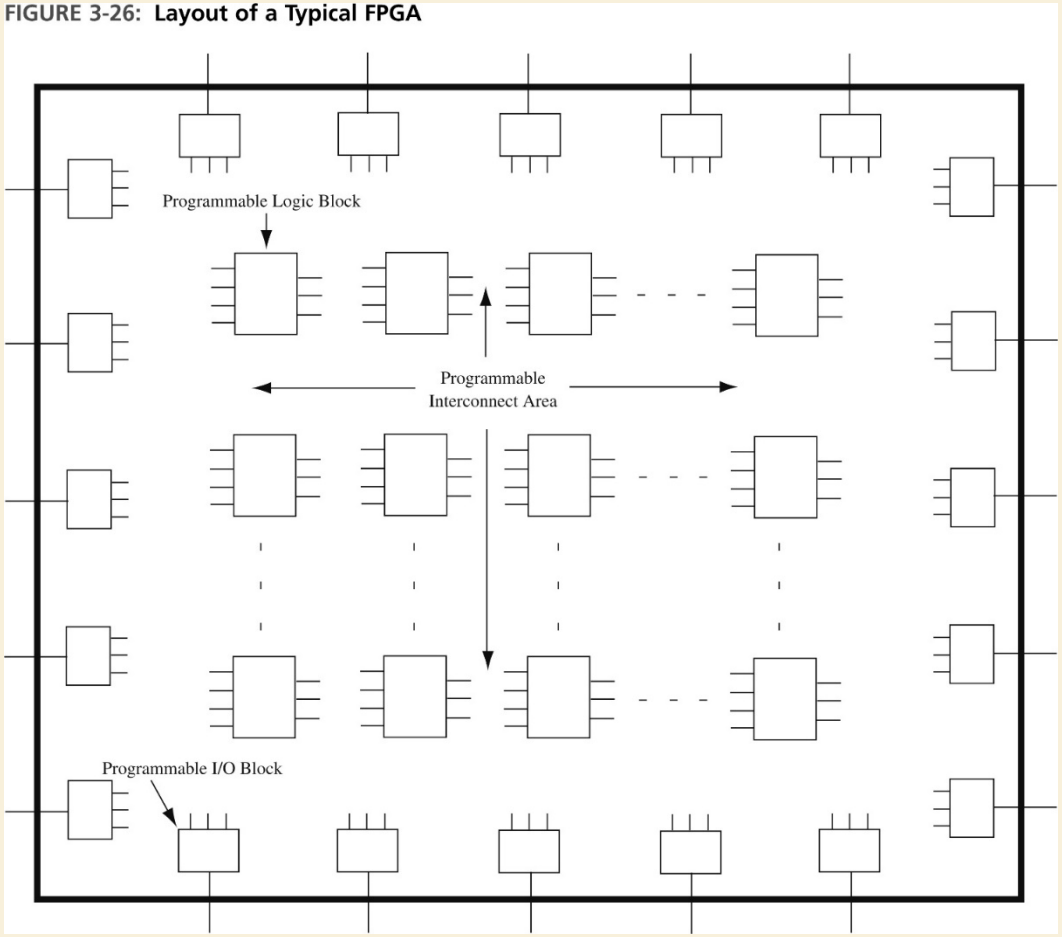
Programmable logic taxonomy



Lab Device

Field Programmable Gate Arrays

FIGURE 3-26: **Layout of a Typical FPGA**



Typical Complexity = 5M – 1B transistors

Basic FPGA Operation

- Writing configuration memory ⇒ defines system function
  - Input/Output Cells
  - Logic in PLBs
  - Connections between PLBs & I/O cells
- Changing configuration memory data ⇒ changes system function
  - Can change at anytime
  - Even while system function is in operation

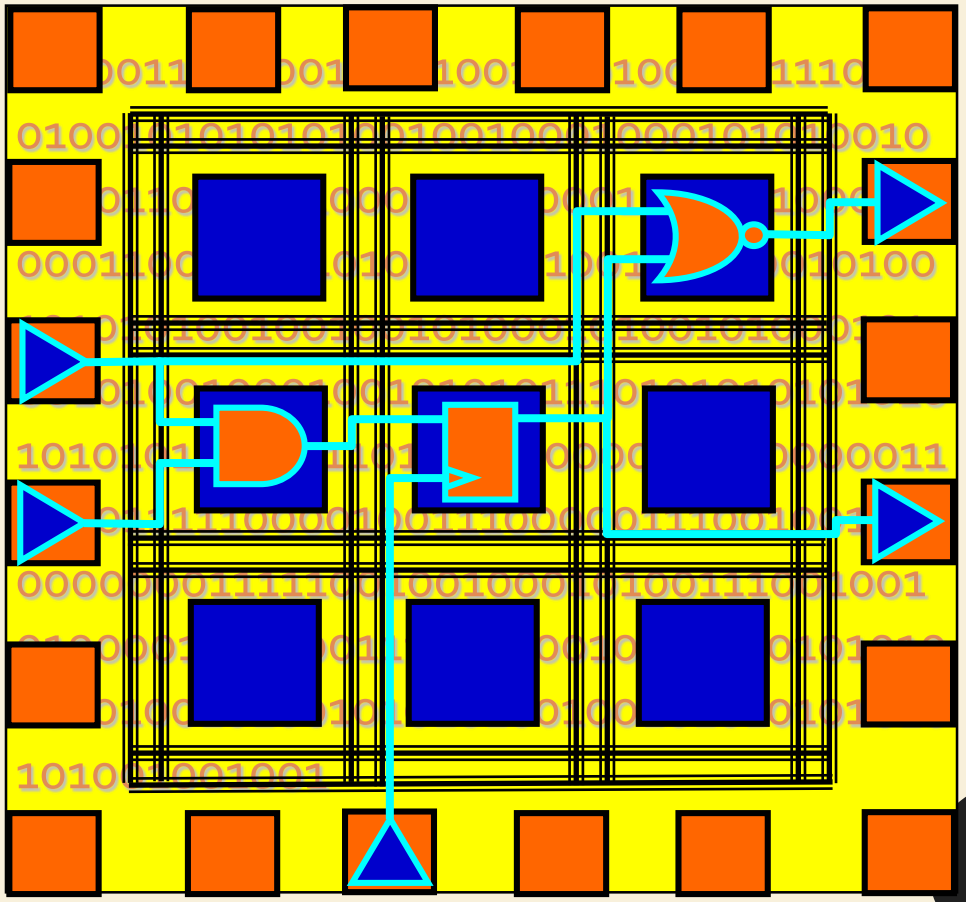


FIGURE 3-27: Typical Architectures for FPGAs

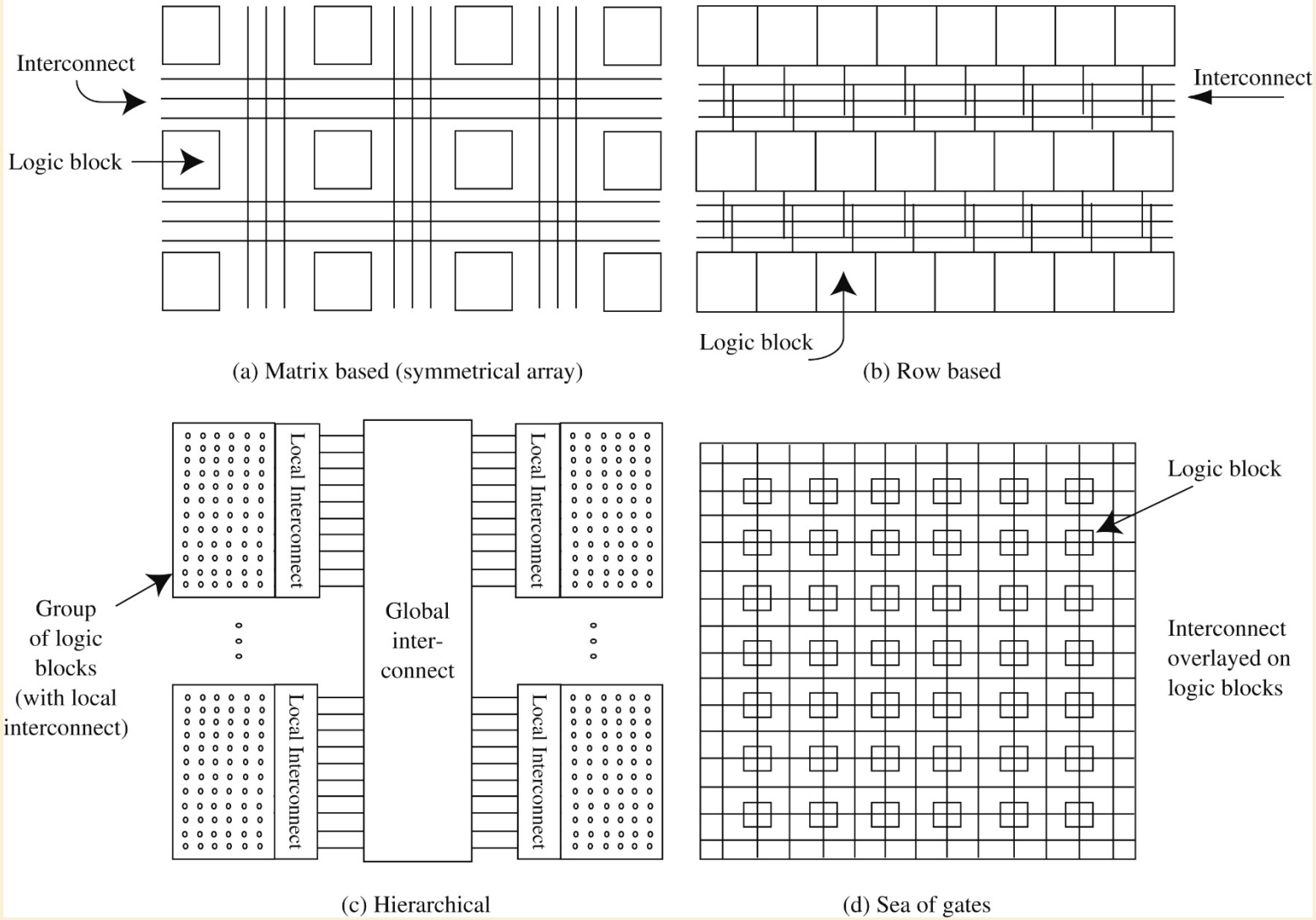


TABLE 3-9: Architecture, Technology, and Logic Block Types of Commercial FPGAs

Company	Device Names	General Architecture	Logic Block Type	Programming Technology
Actel	ProASIC/ProASIC3/ ProASIC^{plus}	Sea of Tiles	Multiplexers & Basic Gates	SRAM
	SX/SXA/eX/MX	Sea of Modules	Multiplexers & Basic Gates	Antifuse
	Accelerator	Sea of Modules	Multiplexers & Basic Gates	SRAM
	Fusion	Sea of Tiles	Multiplexers & Basic Gates	Flash, SRAM
Xilinx	Virtex	Symmetrical Array	LUT	SRAM
	Spartan	Symmetrical Array	LUT	SRAM
Atmel	AT40KAL	Cell Based	Multiplexers & Basic Gates	SRAM
QuickLogic	Eclipse II	Flexible Clock	LUT	SRAM
	PolarPro	Cell Based	LUT	SRAM
Altera	Cyclone II	Two-Dimensional Row and Column Based	LUT	SRAM
	Stratix II	Two-Dimensional Row and Column Based	LUT	SRAM
	APEX II	Row and Column, but Hierarchical Interconnect	LUT	SRAM

Ranges of Resources

FPGA Resource		Small FPGA	Large FPGA
Logic	PLBs per FPGA	256	25,920
	LUTs and flip-flops per PLB	1	8
Routing	Wire segments per PLB	45	406
	PIPs per PLB	139	3,462
Specialized Cores	Bits per memory core	128	36,864
	Memory cores per FPGA	16	576
	DSP cores	0	512
Other	Input/output cells	62	1,200
	Configuration memory bits	42,104	79,704,832

Programmable ASIC logic cells

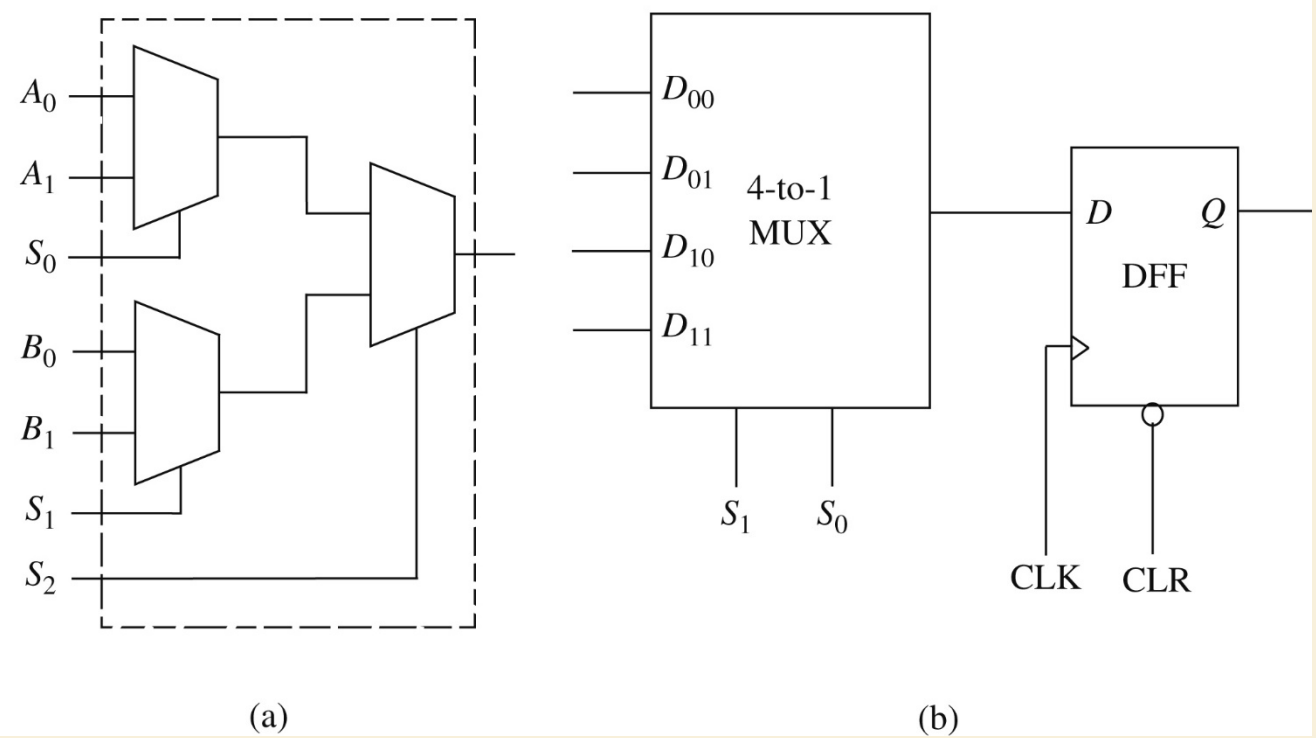
- Xilinx : "configurable logic block" (CLB) contains
  - SRAM lookup tables (LUTs) to implement combinational logic
  - D flip flops
  - Multiplexers to establish paths in the CLB
- Actel "ACT" : multiplexers implement logic
- Altera "Flex" : similar to Xilinx CLB
- Altera "MAX" : PALs implement logic

TABLE 3-8: Characteristics of the Major FPGA Programming Technologies

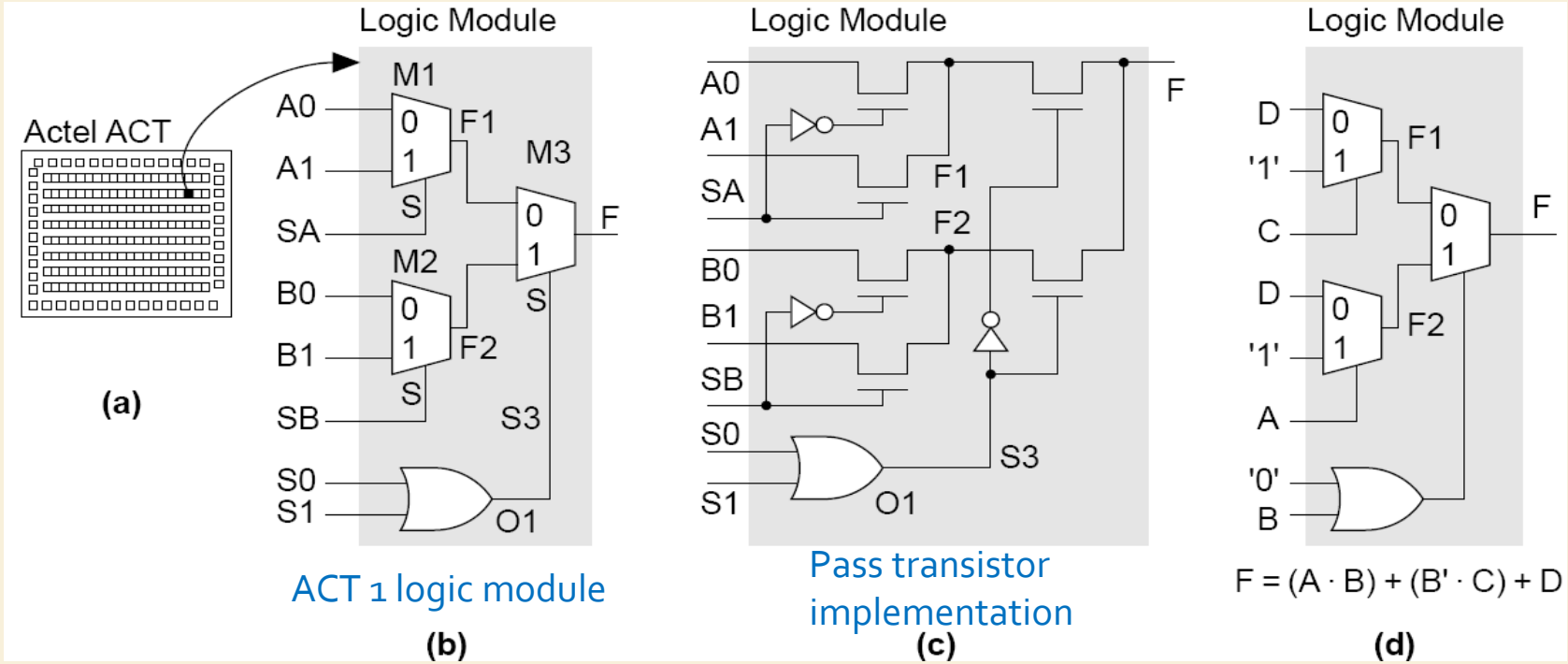
Programming Technology	Volatility	Programmability	Area Overhead	Resistance	Capacitance
SRAM	Volatile	In-circuit reprogrammable	Large	Medium to high	High
EPROM	Nonvolatile	Out-of-circuit reprogrammable	Small	High	High
EEPROM	Nonvolatile	In-circuit reprogrammable	Medium to high	High	High
Antifuse	Nonvolatile	Not reprogrammable	Small	Small	Small

Mux-based logic blocks in FPGAs

Text Figure 3.33



Actel ACT architecture (Fig. 5.1)
(mux-based logic modules)



Xilinx FPGA families (2015)

	Spartan-6	Artix-7	Kintex-7	Virtex-7	Kintex UltraScale	Virtex UltraScale
Logic Cells	147,443	215,360	477, 760	1,954,560	1,160,880	4,432,680
BlockRAM	4.8Mb	13Mb	34Mb	68Mb	76Mb	132.9Mb
DSP Slices	180	740	1,920	3,600	5,520	2,880
DSP Performance (symmetric FIR)	140GMACs	930GMACs	2,845GMACs	5,335GMACs	8,180 GMACs	4,268 GMACs
Transceiver Count	8	16	32	96	64	120
Transceiver Speed	3.2 Gb/s	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s	16.3 Gb/s	32.75 Gb/s
Total Transceiver Bandwidth (full duplex)	50 Gb/s	211 Gb/s	800 Gb/s	2,784 Gb/s	2,086 Gb/s	5,886 Gb/s
Memory Interface (DDR3)	800	1,066	1,866	1,866	2,400	2,400
PCI Express® Interface	x1 Gen1	x4 Gen2	x8 Gen2	x8 Gen3	x8 Gen3	x8 Gen3
Analog Mixed Signal (AMS)/XADC	-	XADC	XADC	XADC	System Monitor	System Monitor
Configuration AES	Yes	Yes	Yes	Yes	Yes	Yes
I/O Pins	576	500	500	1,200	832	1,456
I/O Voltage	1.2V – 3.3V	1.2V – 3.3V	1.2V – 3.3V	1.2V – 3.3V	1.0 – 3.3V	1.0 – 3.3V

Digikey.com (4/03/18):

Spartan-3A XC3S50A: $8.05

Spartan-6 XC6SLX4: $11.48

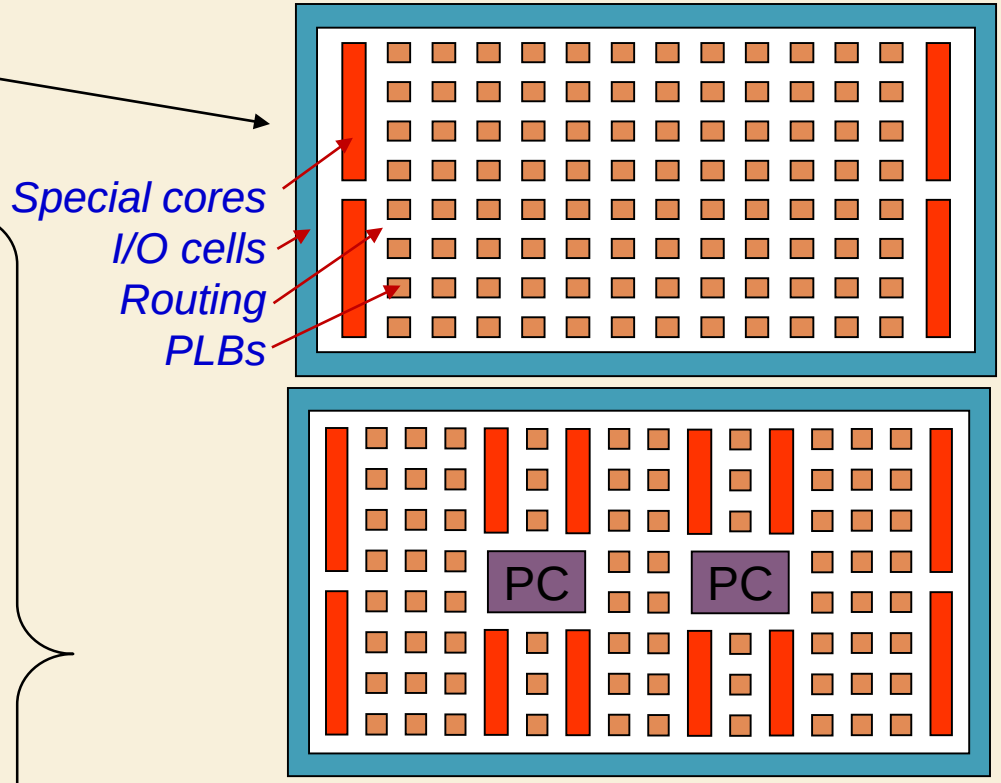
Artix-7 XC7A100T: $136.50

Kinetix-7 XC7K70T: $139.65

Virtex7 XC7V1140T-G2FLG1925E: $32,815.17

Xilinx FPGAs

- Virtex and Spartan 2
  - Array of 96 to 6,144 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 FF/latches
  - 4 to 32 4K-bit dual-port RAMs
- Virtex II, Virtex II Pro
  - Array of 352 to 11,204 PLBs
    - 8 LUTs/RAMs (4-input)
    - 8 FF/latches
  - 12 to 444 18K-bit dual-port RAMs
  - 12 to 444 18×18-bit multipliers
  - 0 to 2 PowerPC processor cores
- Virtex 4
  - Array of 1,536 to 22,272 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 LUTs (4-input)
    - 8 FF/latches
  - 48 to 552 18K-bit dual-port RAMs
    - Also operate as FIFOs
  - 32 to 512 DSP cores include:
  - 0 to 2 PowerPC processor cores



- Spartan 3
  - Array of 192 to 8,320 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 LUTs (4-input)
    - 8 FF/latches
  - 4 to 104 18K-bit dual-port RAMs
  - 4 to 104 18×18-bit multipliers

Xilinx 7 Series Families

Maximum Capability	Artix-7 Family	Kintex-7 Family	Virtex-7 Family
Logic Cells	215K	478K	1,955K
Block RAM(1)	13 Mb	34 Mb	68 Mb
DSP Slices	740	1,920	3,600
Peak DSP Performance(2)	929 GMAC/s	2,845 GMAC/s	5,335 GMAC/s
Transceivers	16	32	96
Peak Transceiver Speed	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Peak Serial Bandwidth (Full Duplex)	211 Gb/s	800 Gb/s	2,784 Gb/s
PCIe Interface	x4 Gen2	x8 Gen2	x8 Gen3
Memory Interface	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	500	500	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Package Options	Low-Cost, Wire-Bond, Lidless Flip-Chip	Low-Cost, Lidless Flip-Chip and High-Performance Flip-Chip	Highest Performance Flip-Chip

Xilinx Artix-7 Family

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTPs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7A15T	16,640	2,600	200	45	50	25	900	5	1	4	1	5	250
XC7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A75T	75,520	11,800	892	180	210	105	3,780	6	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Artix-7 FPGA Interface Blocks for PCI Express support up to x4 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTP transceivers.

Package[1]	CPG236		CSG324		CSG325		FTG256		SBG484 SBV484		FGG484[2]		FBG484[2] FBV484		FGG676[3]		FBG676[3] FBV676		FFG1156 FFV1156	
Size (mm)	10 x 10		15 x 15		15 x 15		17 x 17		19 x 19		23 x 23		23 x 23		27 x 27		27 x 27		35 x 35	
Ball Pitch (mm)	0.5		0.8		0.8		1.0		0.8		1.0		1.0		1.0		1.0		1.0	
Device	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]
XC7A15T	2	106	0	210	4	150	0	170			4	250								
XC7A35T	2	106	0	210	4	150	0	170			4	250								
XC7A50T	2	106	0	210	4	150	0	170			4	250								
XC7A75T			0	210			0	170			4	285			8	300				
XC7A100T			0	210			0	170			4	285			8	300				
XC7A200T									4	285			4	285			8	400	16	500

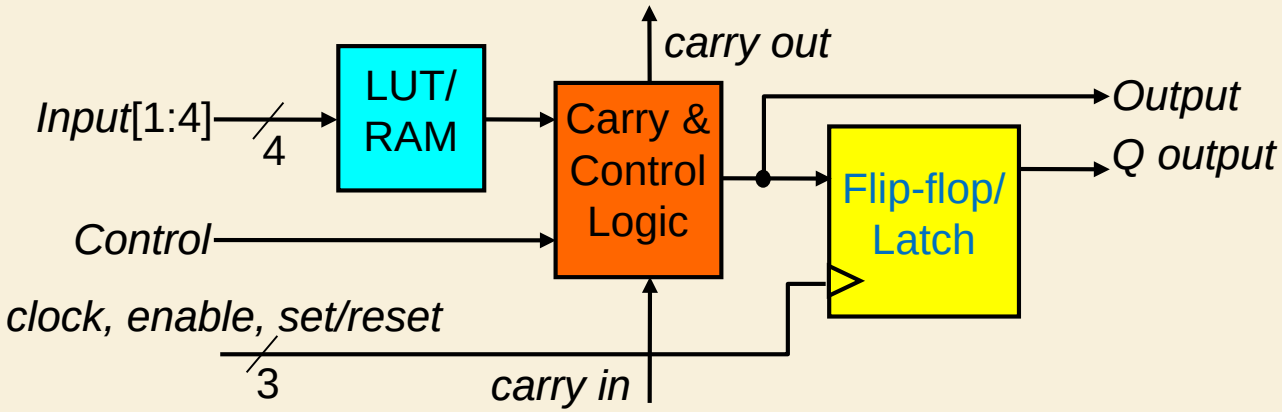
Xilinx "UltraScale" Family

Kintex and Virtex UltraScale and UltraScale+

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K)	318–1,451	356–1,143	783–5,541	862–3,780	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–34.6	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–36		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–8		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	2,280–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	32.75	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–832	82–668	280–408

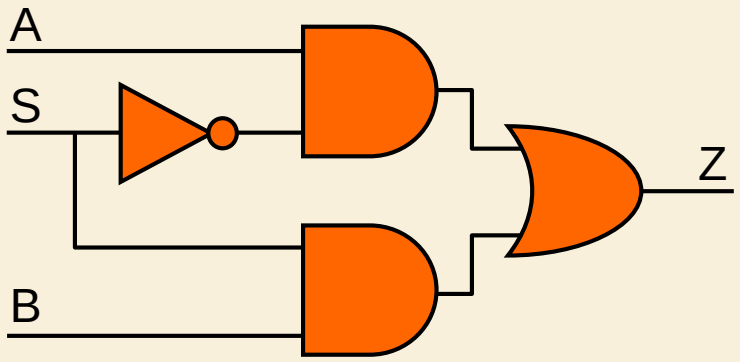
Xilinx: Basic CLB Architecture

- Look-up Table (LUT) implements truth table
- Memory elements:
  - Flip-flop/latch
  - Some FPGAs - LUTs can also implement small RAMs
- Carry & control logic implements fast adders/subtractors



Combinational Logic Functions

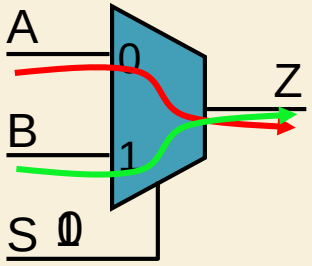
- Gates are combined to create complex circuits
- Multiplexer example
  - If S = 0, Z = A
  - If S = 1, Z = B
  - Very common digital circuit
  - Heavily used in FPGAs
    - S input controlled by configuration memory bit
    - We'll see it again



Truth table

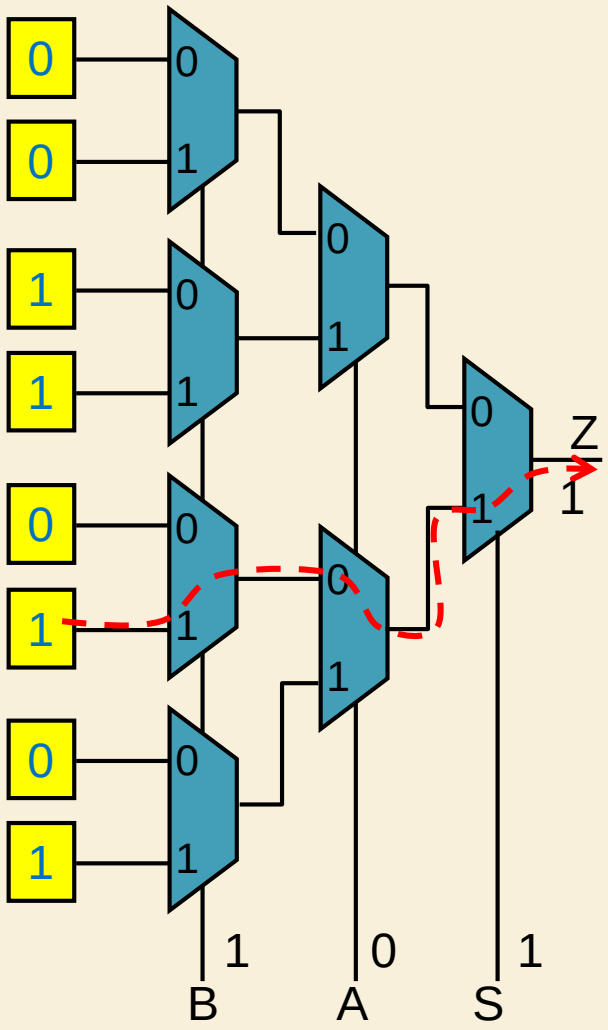
S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Logic symbol

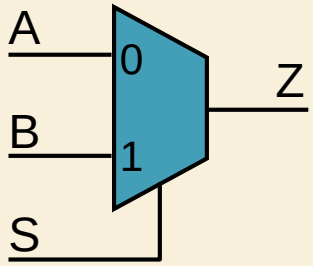


Look-up Tables

- Recall multiplexer example
- Configuration memory holds outputs for truth table
- Internal signals connect to control signals of multiplexers to select value of truth table for any given input value



Multiplexer



Truth table

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Look-up Table Based RAMs

- Functions of more variables than LUT inputs

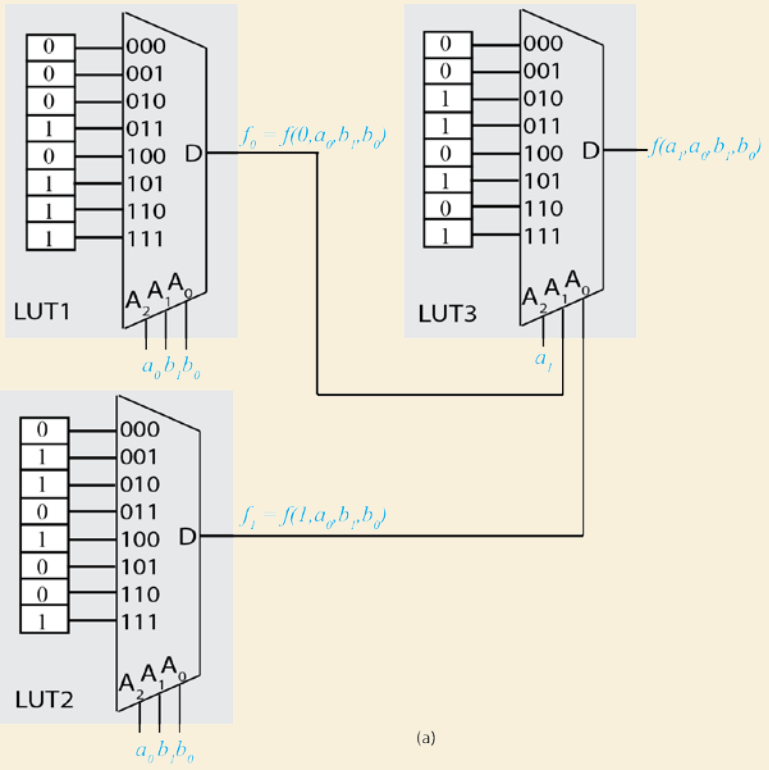
$$f(a_1, a_0, b_1, b_0) = a_1 f(1, a_0, b_1, b_0) + a_1' f(0, a_0, b_1, b_0)$$

$a_1 a_0$	$b_1 b_0$	$f(a_1, a_0, b_1, b_0)$	
0	0 0 0	0	$f(0, a_0, b_1, b_0) = f_0$
0	0 0 1	1	
0	0 1 0	1	
0	0 1 1	1	
0	1 0 0	0	
0	1 0 1	0	
0	1 1 0	1	
0	1 1 1	1	
1	0 0 0	0	$f(1, a_0, b_1, b_0) = f_1$
1	0 0 1	0	
1	0 1 0	0	
1	0 1 1	1	
1	1 0 0	0	
1	1 0 1	0	
1	1 1 0	0	
1	1 1 1	0	

(a)

a_1	f_0	f_1	$f(a_1, a_0, b_1, b_0)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

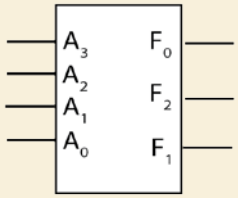
(b)

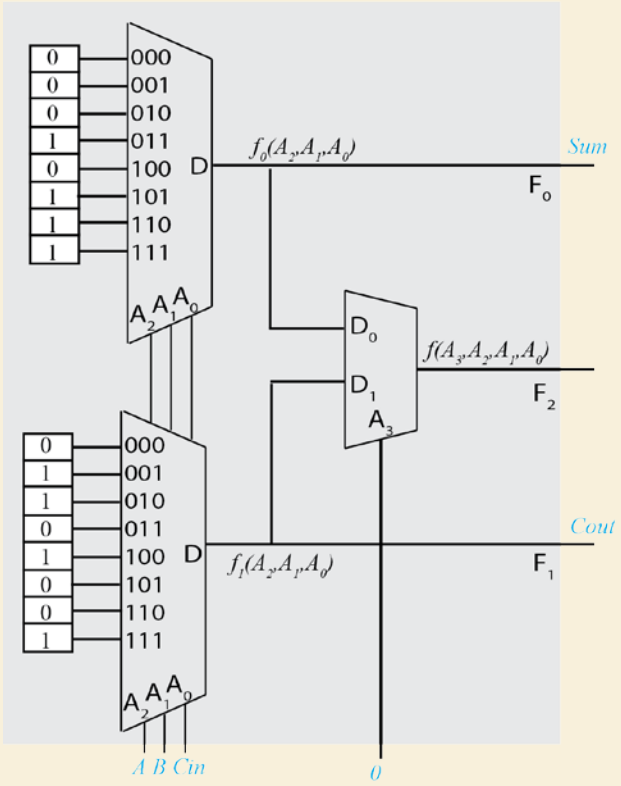


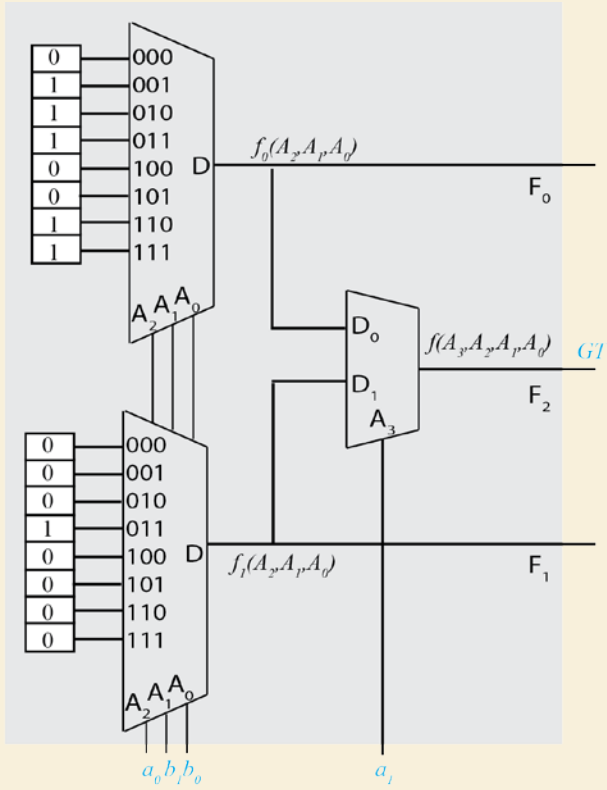
(a)

Look-up Table Based RAMs

- Artix-7 6-input LUTs can be partitioned into two 5-input LUTs

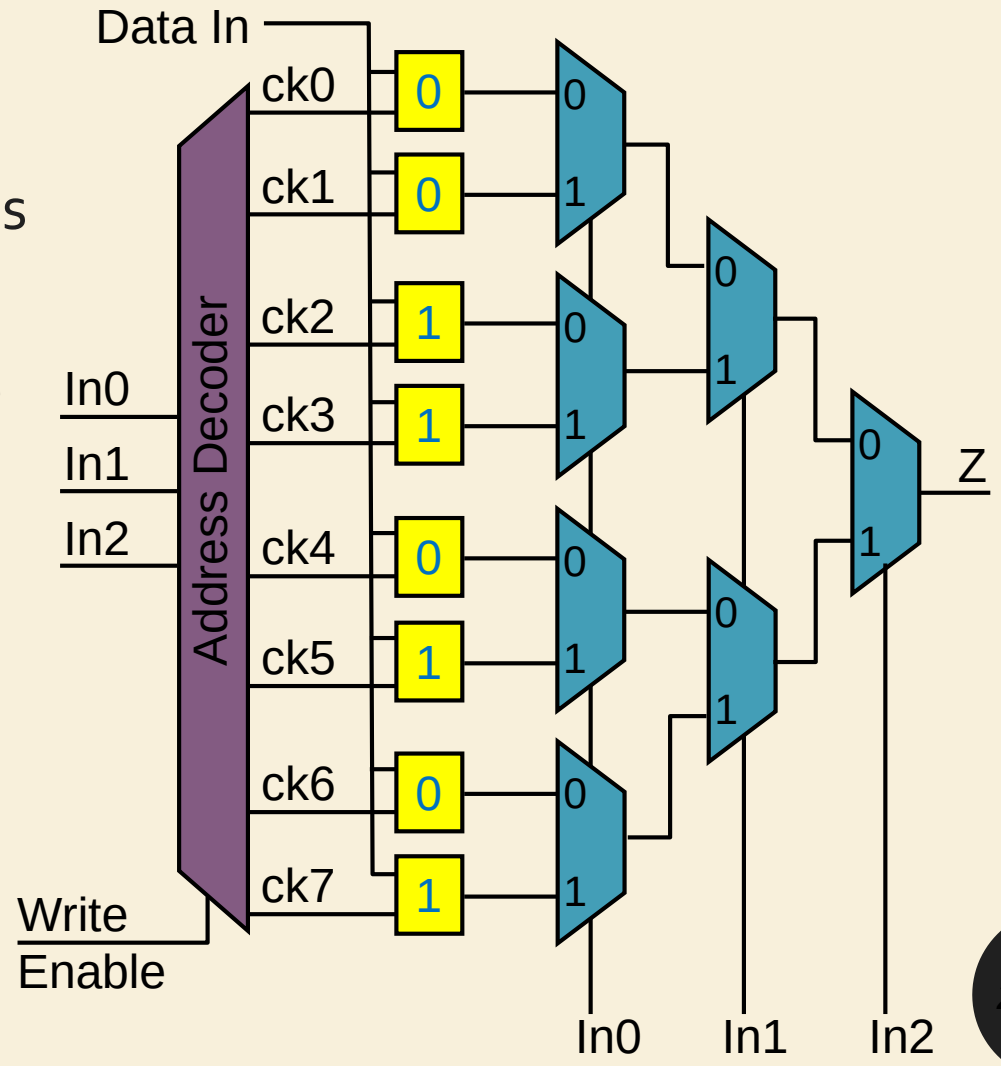






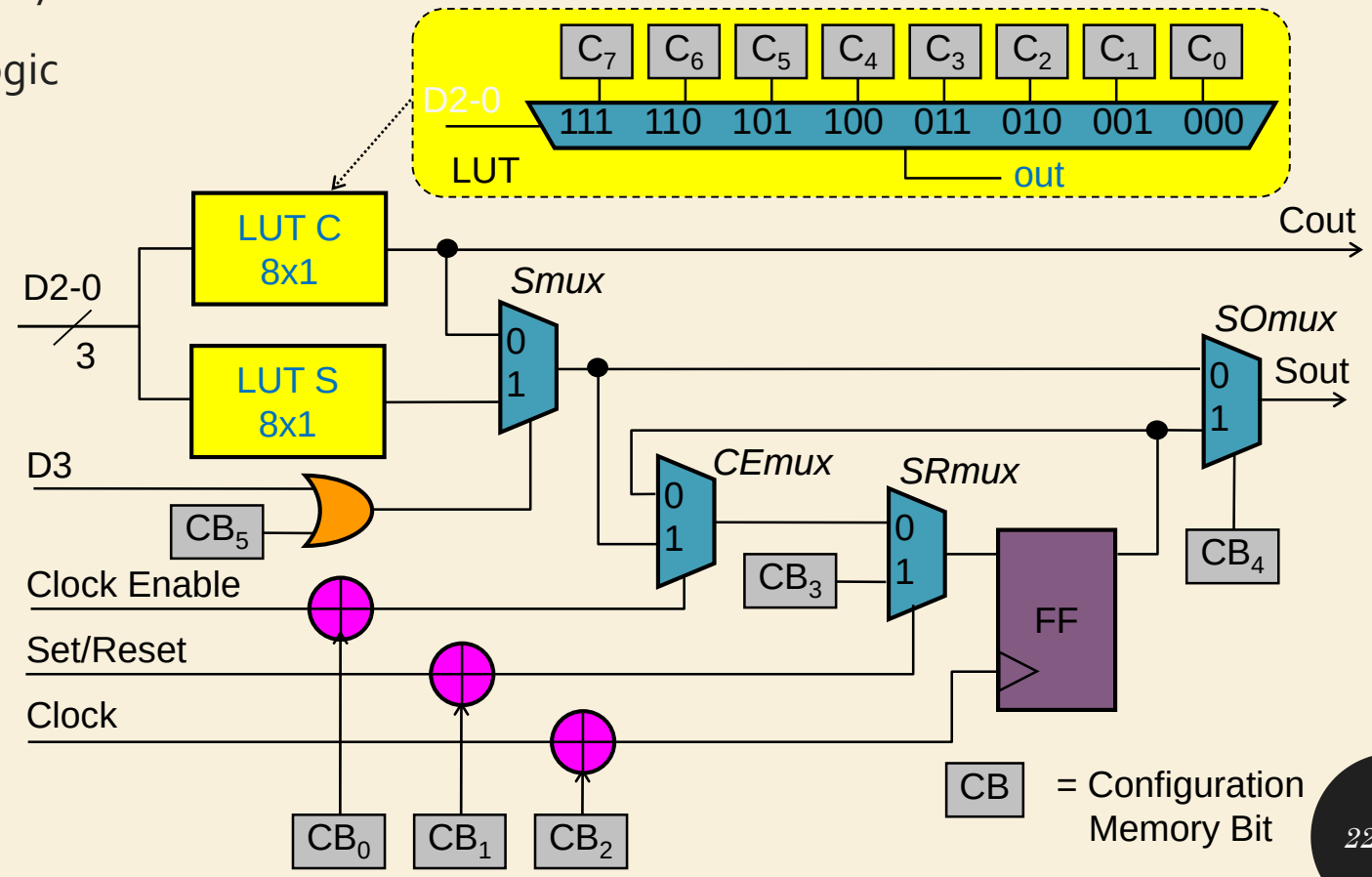
Look-up Table Based RAMs

- Normal LUT mode performs read operations
- Address decoder with write enable generates clock signals to latches for write operations
- Small RAMs but can be combined for larger RAMs



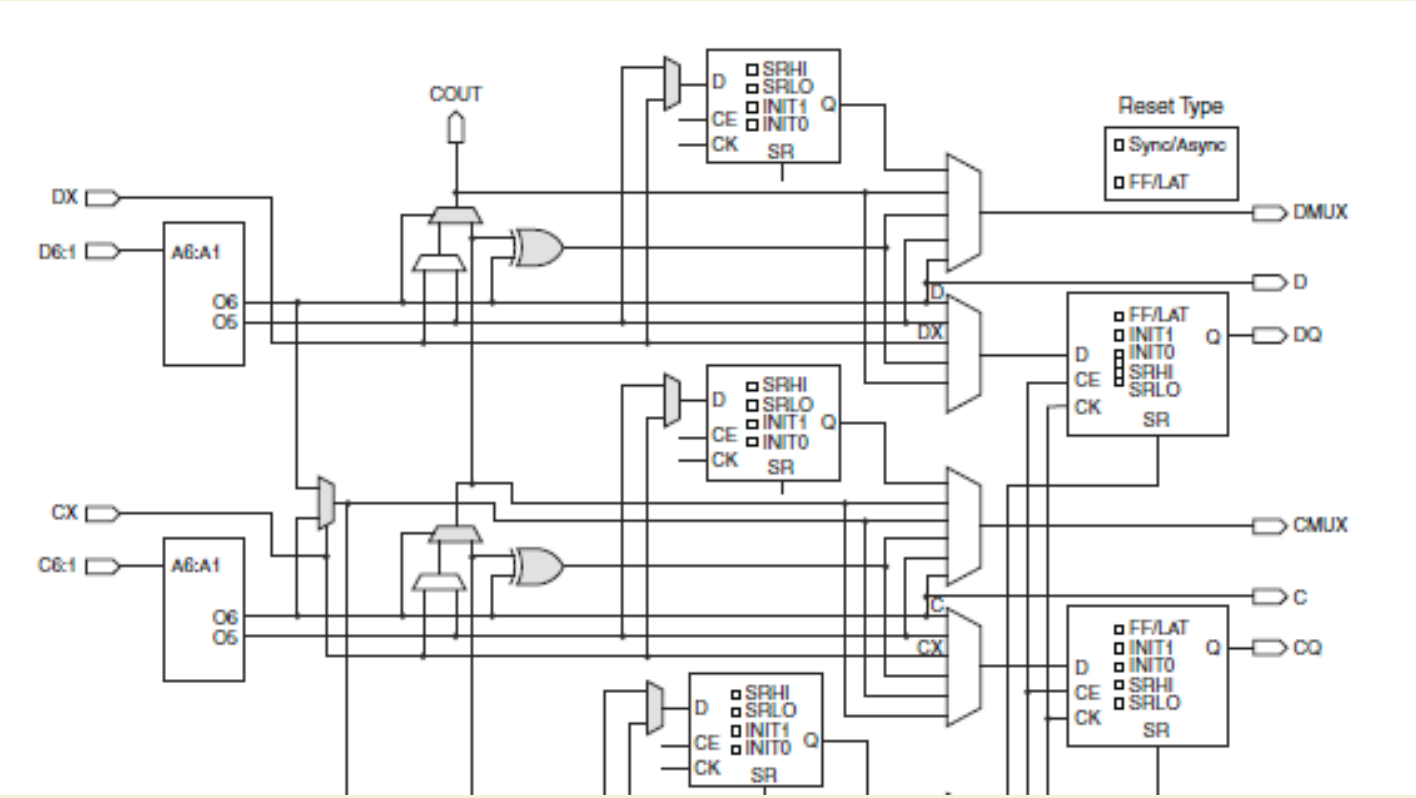
A Simple CLB

- Two 3-input LUTs
  - Can implement any 4-input combinational logic function
- 1 flip-flop
  - Programmable:
    - Active levels
    - Clock edge
    - Set/reset
- 22 configuration memory bits
  - 8 per LUT
    - Co-7
    - So-7
  - 6 controls
    - CBo-7

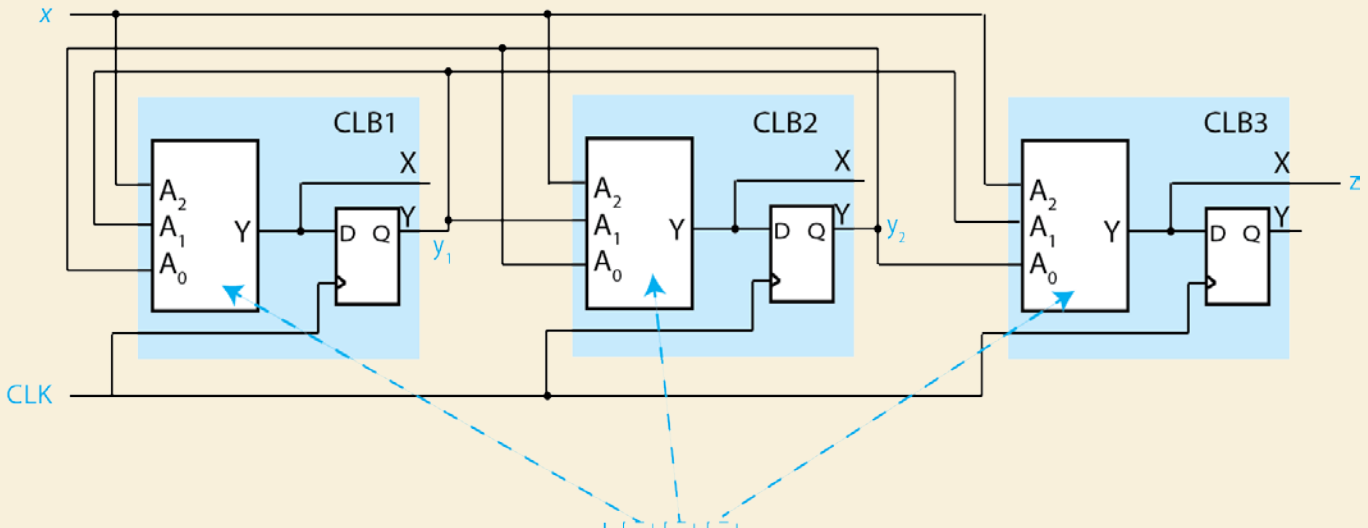


Example CLB

- Artix-7 SLICEL (1/2 shown)
- Four 6-input Look-Up Tables (LUTs)
  - Any combinational logic function of up to 6 inputs
  - SLICEM LUT can function as small RAM (16x1-bit) or shift register (up to 16-bit)
- Eight D flip-flops
  - Programmable as latches
  - Programmable clock edge, clock enable, set/reset
- Extra logic
  - Fast carry for adders
  - MUXs for Shannon expansion
  - And more



Synchronous sequential circuit



x

State	0	1
A	A/0	B/0
B	A/0	C/1
C	B/0	D/0
D	C/1	D/0

Next State/Output

State	y_1	y_2
A	0	0
B	0	1
C	1	1
D	1	0

x

$y_1 y_2$	0	1
00	00/0	01/0
01	00/0	11/1
11	01/0	10/0
10	11/1	10/0

$Y_1 Y_2/z$

$x\, y_1 y_2$	Y_1	Y_2	z
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	1	1	1
0 1 1	0	1	0
1 0 0	0	1	0
1 0 1	1	1	1
1 1 0	1	0	0
1 1 1	1	0	0

CLBs and Slices in rows/columns

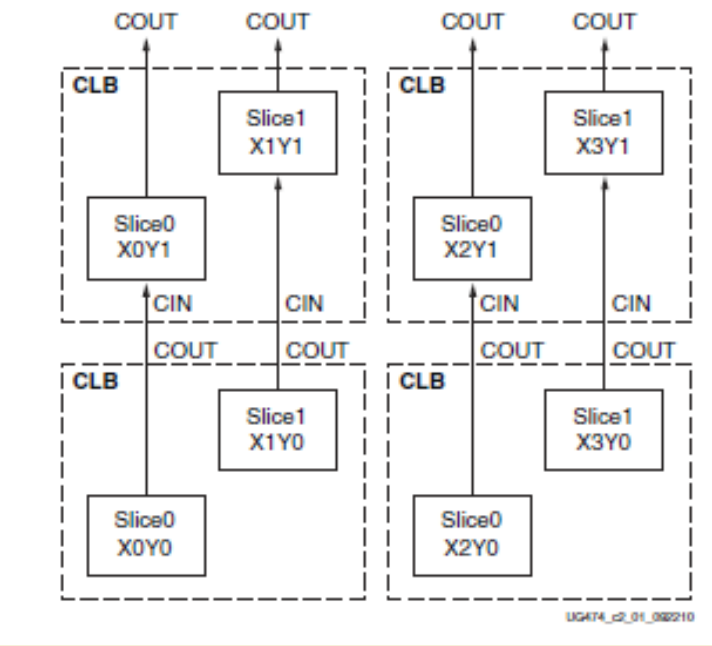


Table 2-1: **Logic Resources in One CLB**

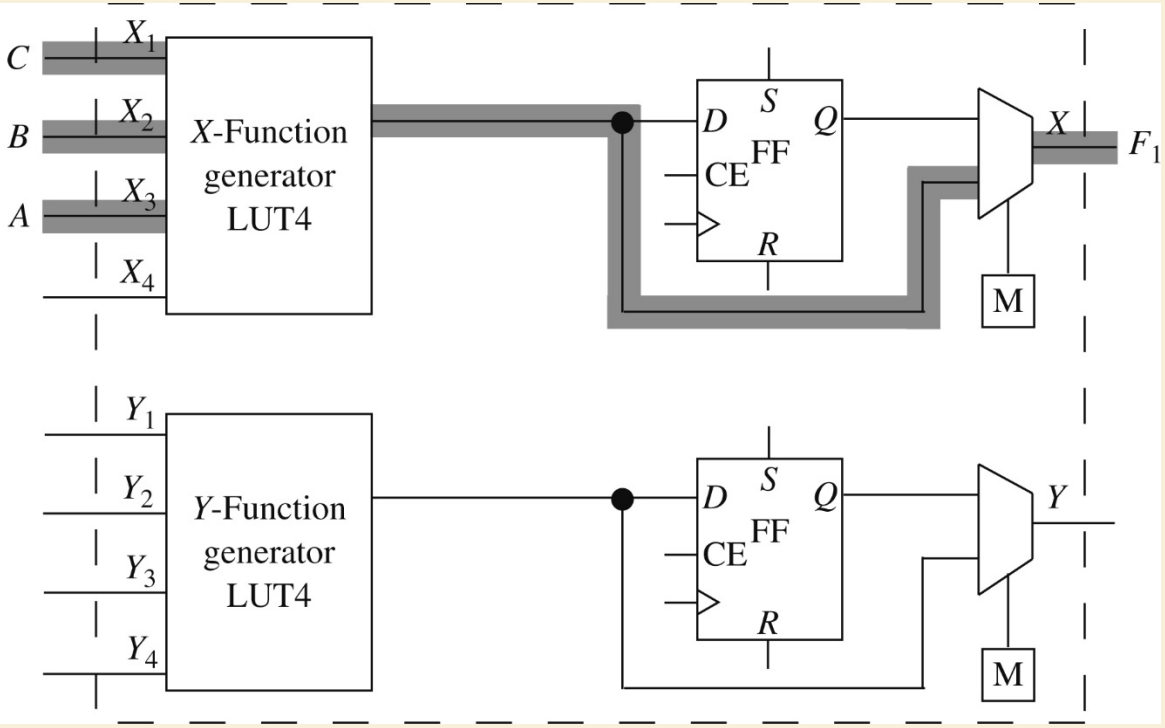
Slices	LUTs	Flip-Flops	Arithmetic and Carry Chains	Distributed RAM(1)	Shift Registers(1)
2	8	16	2	256 bits	128 bits

Notes:

1. SLICEM only, SLICEL does not have distributed RAM or shift registers.

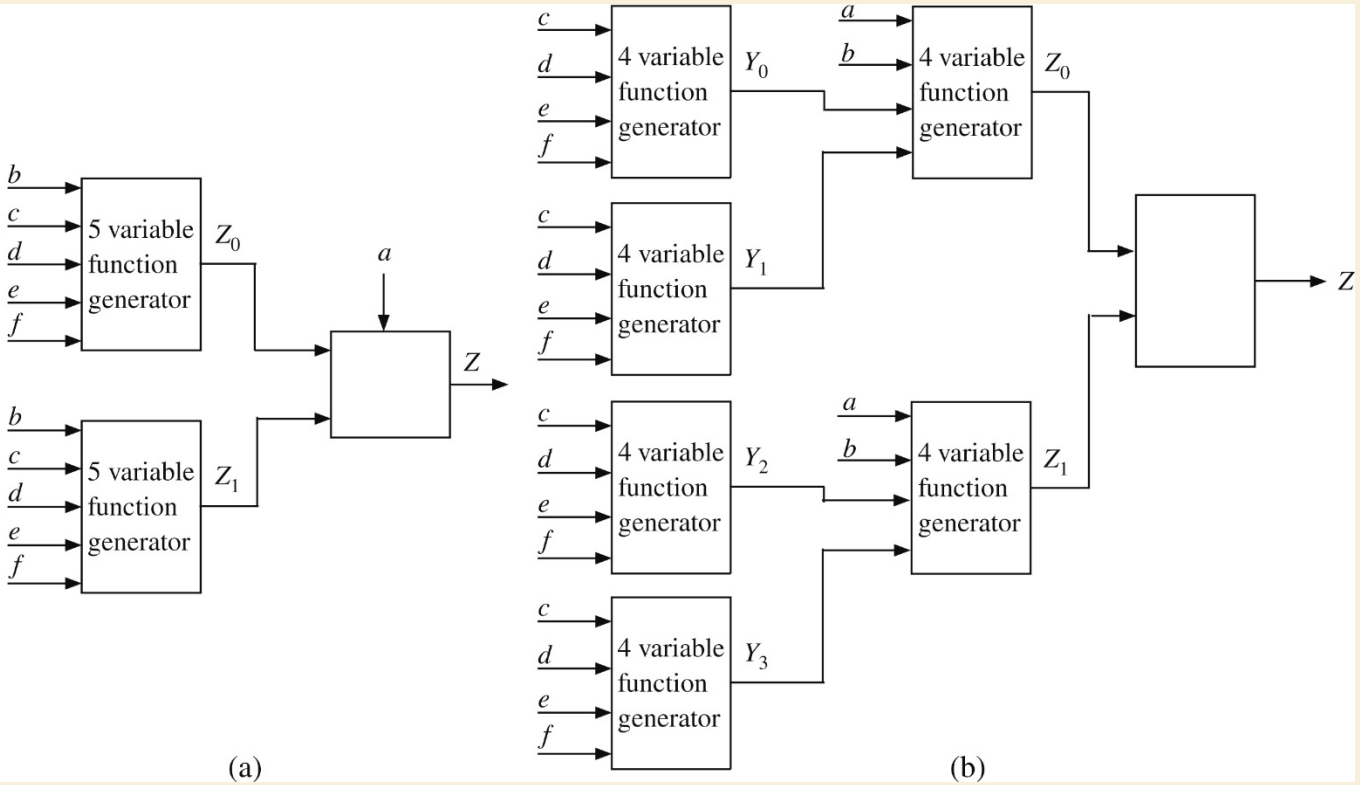
Using lookup-table (LUT) programmable logic

FIGURE 3-32:
Highlighting Paths for Function F_1



Functions of more variables than # of LUT inputs

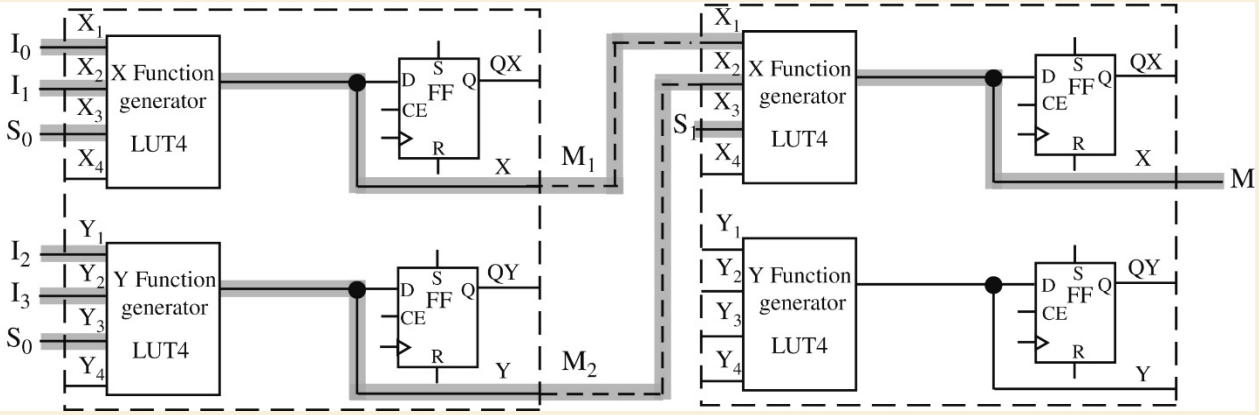
FIGURE 6-6:
Realization of Six-Variable Functions Using (a) Five-Variable and (b) Four-Variable Function Generators



Shannon's Expansion Theorem (partition into smaller functions):

$$Z(a,b,c,d,e,f) = \overline{a} \cdot Z(0,b,c,d,e,f) + a \cdot Z(1,b,c,d,e,f) = \overline{a}Z_0 + aZ_1$$

FIGURE 6-2:
Highlighting Paths for a 4-to-1 Mux



$$M = \underbrace{\overline{S}_1\overline{S}_0 I_0 + \overline{S}_1 S_0 I_1}_{M1} + \underbrace{S_1\overline{S}_0 I_2 + S_1 S_0 I_3}_{M2}$$

FIGURE 6-4:
A 4-to-1 Multiplexer in a Programmable Logic Block with Three Function Generators

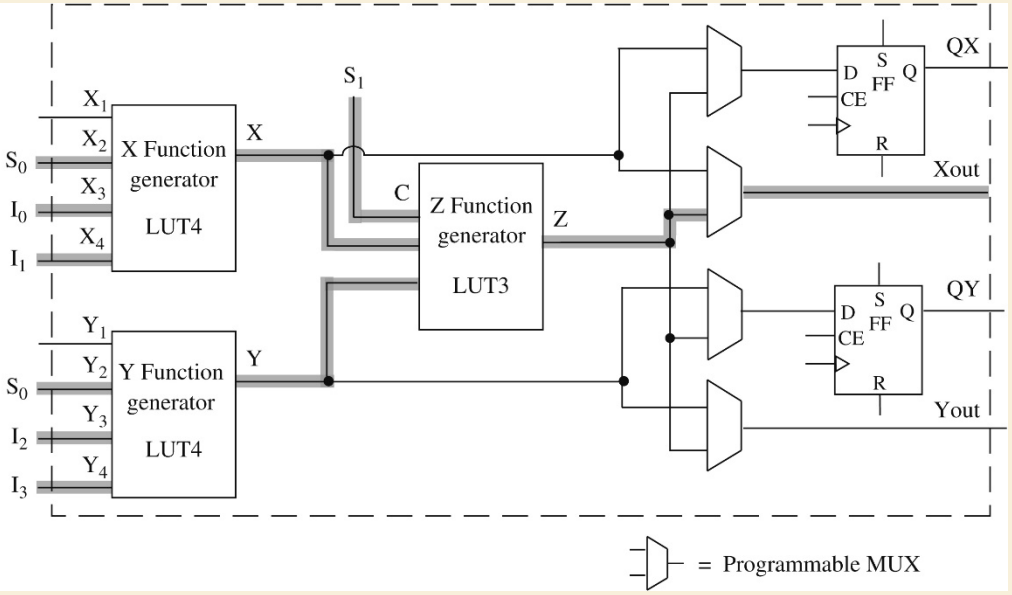


FIGURE 6-5:
(a) Circular Shift Register;
(b) Implementation Using Simple FPGA Building Block

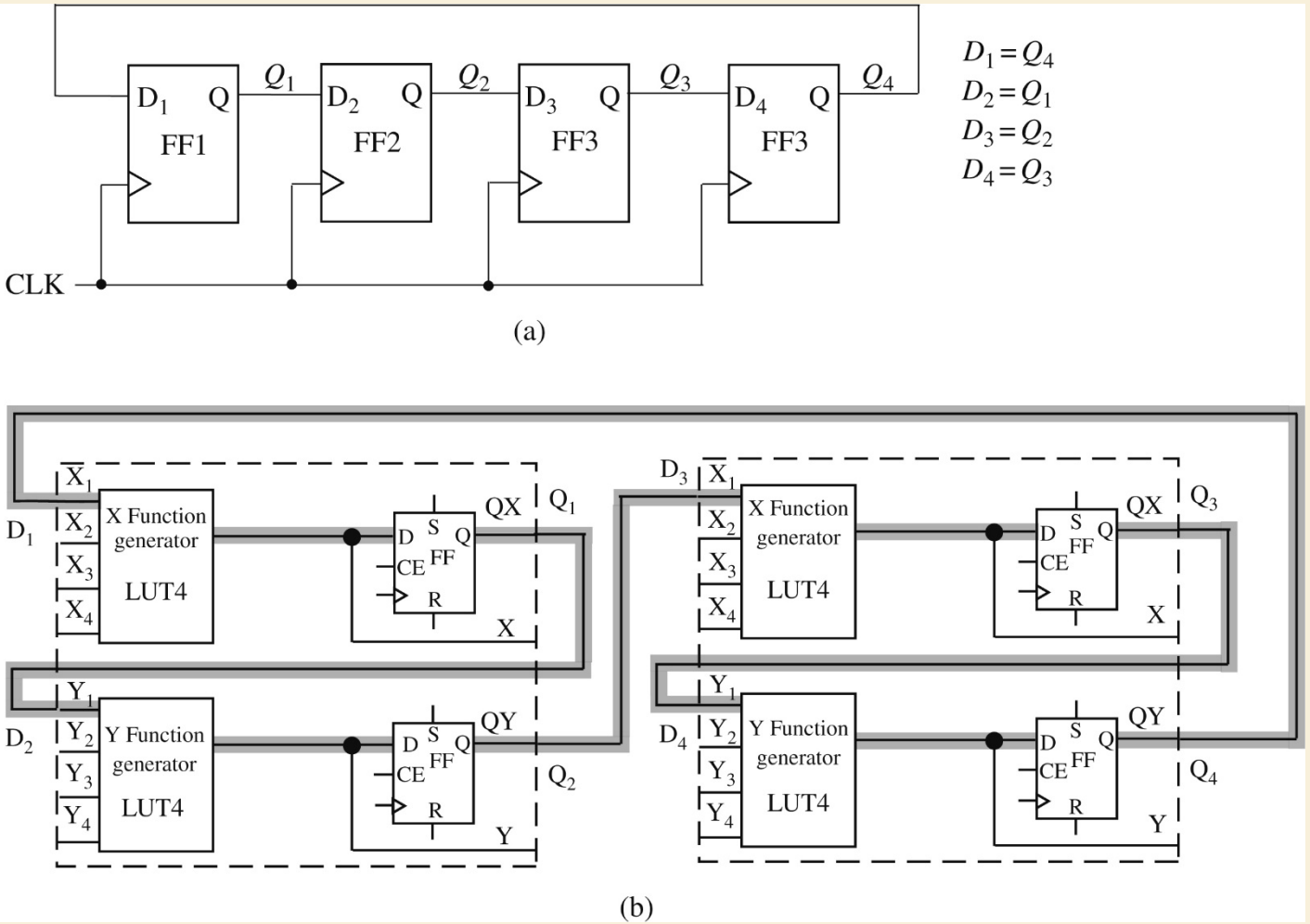


FIGURE 6-11: **Carry Chains for Fast Addition**

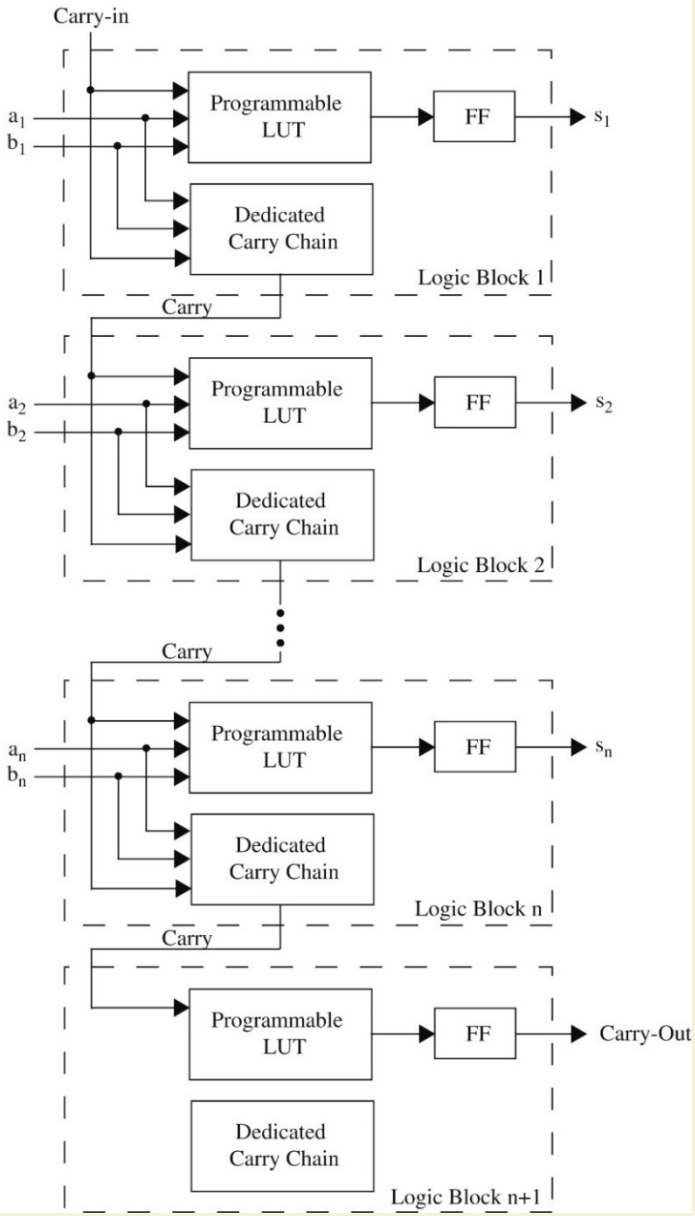
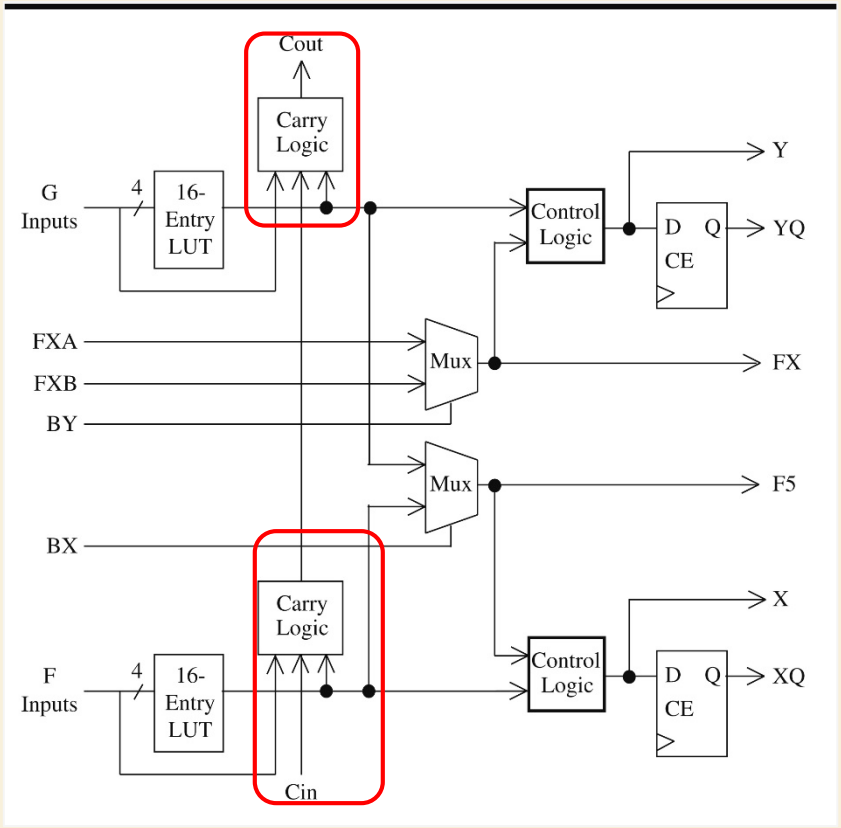
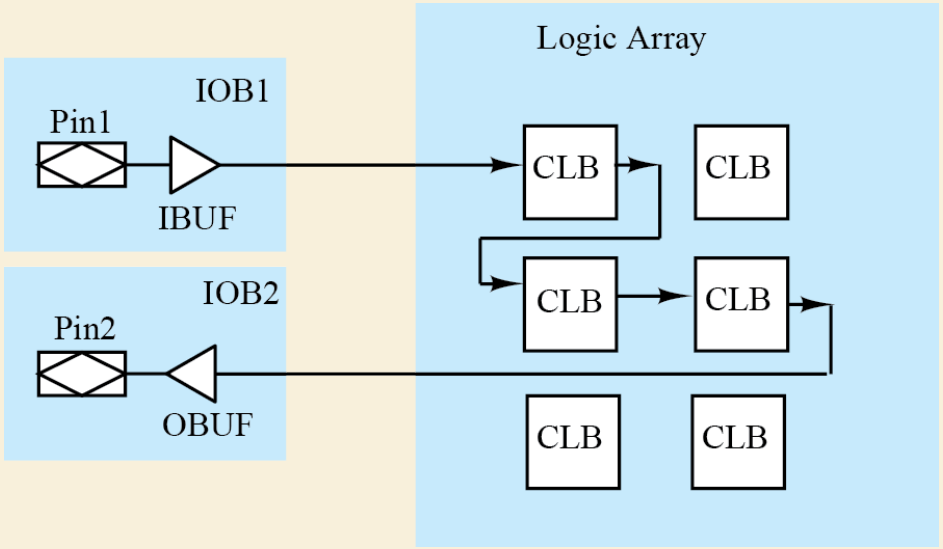


Fig. 6-13 Simplified Spartan and Virtex Slice



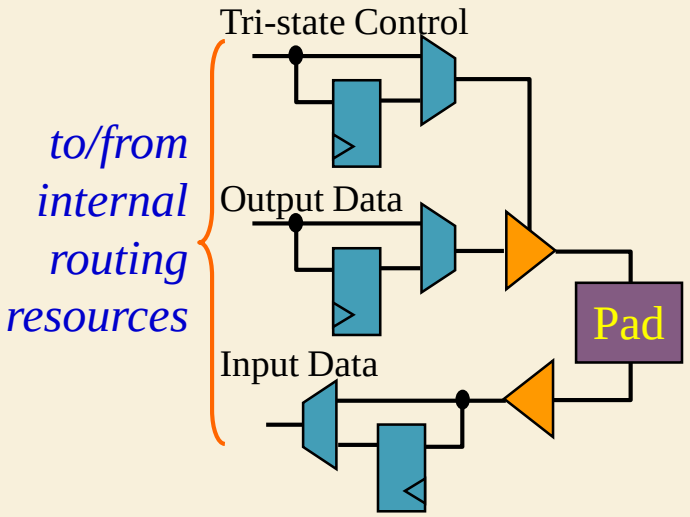
Input/Output Cells

- Signals between I/O pins and the logic array



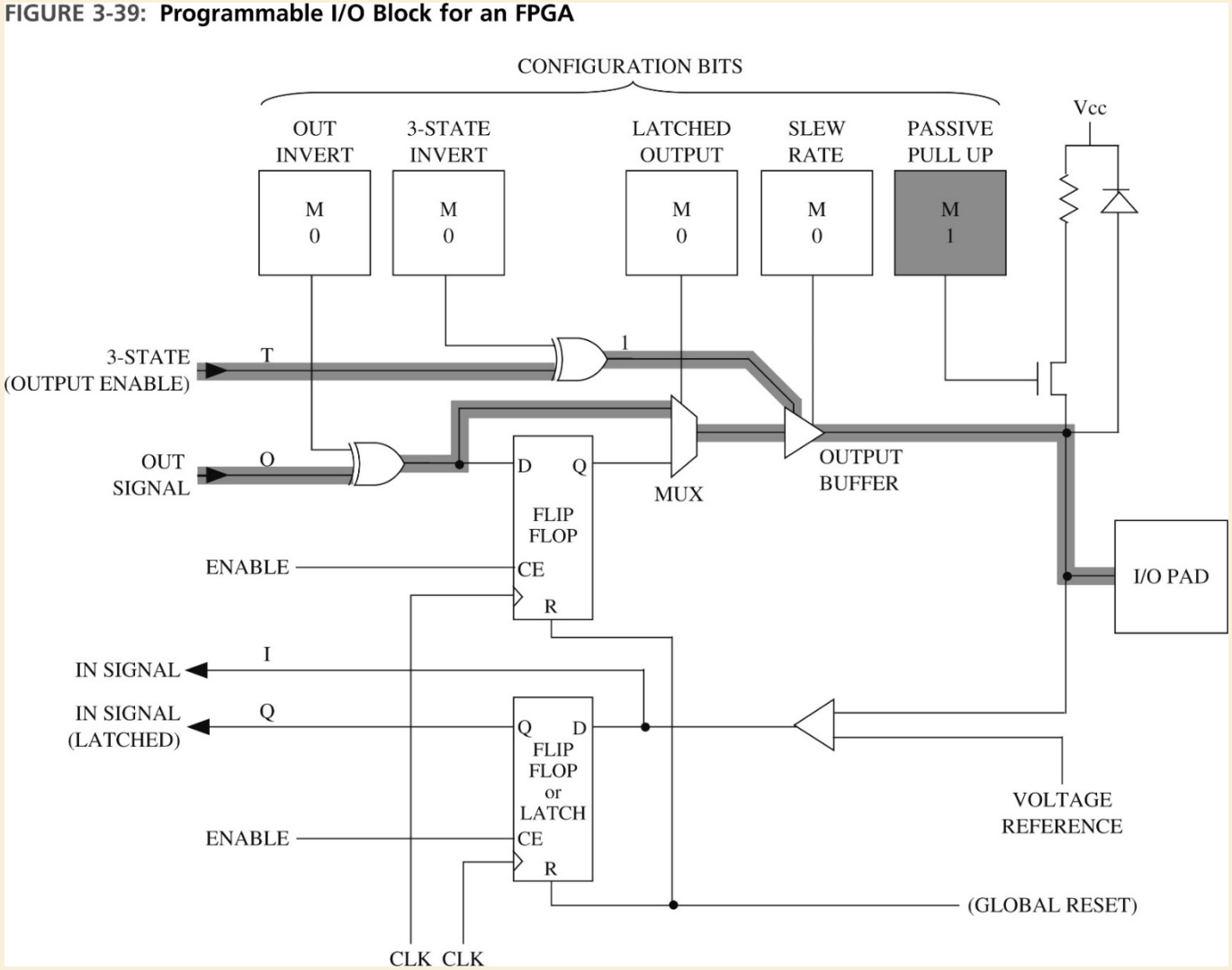
Input/Output Cells

- Bi-directional buffers
  - Programmable for input or output
  - Tri-state control for bi-directional operation
  - Flip-flops/latches for improved timing
    - Set-up and hold times
    - Clock-to-output delay
  - Pull-up/down resistors
- Routing resources
  - Connections to core of array
- Programmable I/O voltage & current levels



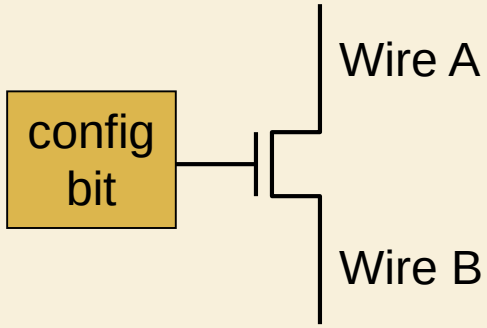
Detailed I/O Cell

FIGURE 3-39: **Programmable I/O Block for an FPGA**

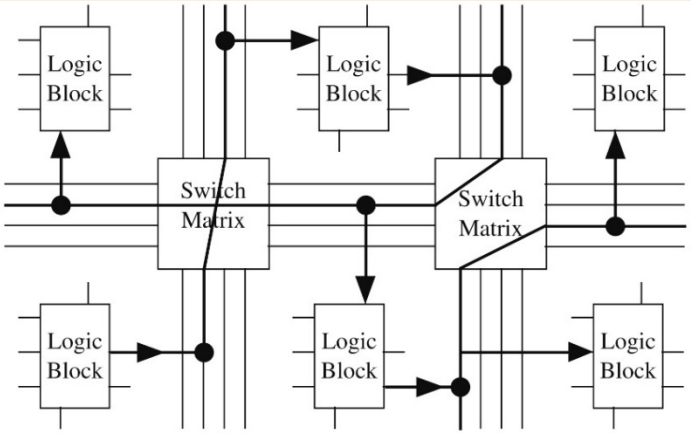


Interconnect Network

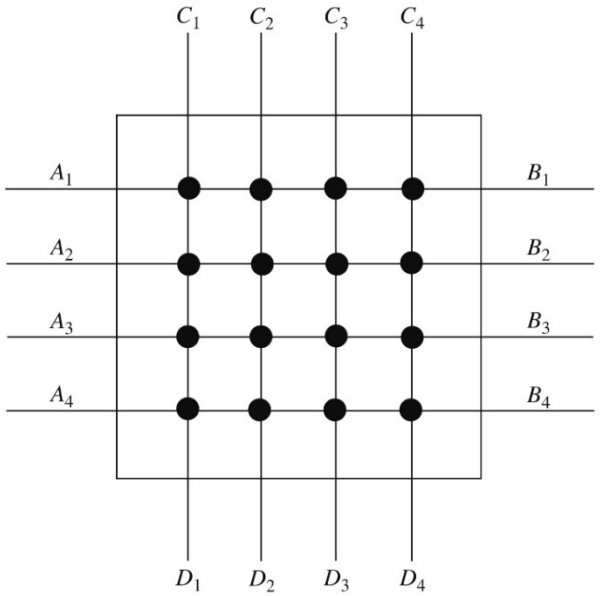
- Wire segments of varying length
  - x*N* = *N* CLBs in length
    - 1, 2, 4, and 6 are most common
  - xH = half the array in length
  - xL = length of full array
- Programmable Interconnect Points (PIPs)
    - Also known as Configurable Interconnect Points (CIPs)
  - Transmission gate connects to 2 wire segments
  - Controlled by configuration memory bit
    - 0 = wires disconnected
    - 1 = wires connected



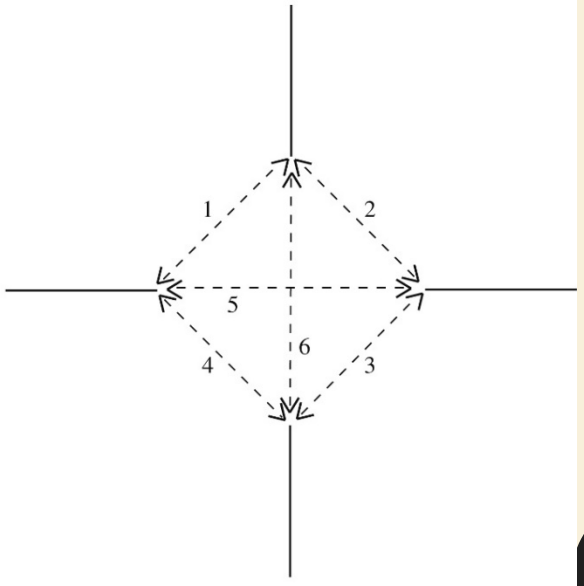
Xilinx interconnect structures



(a)



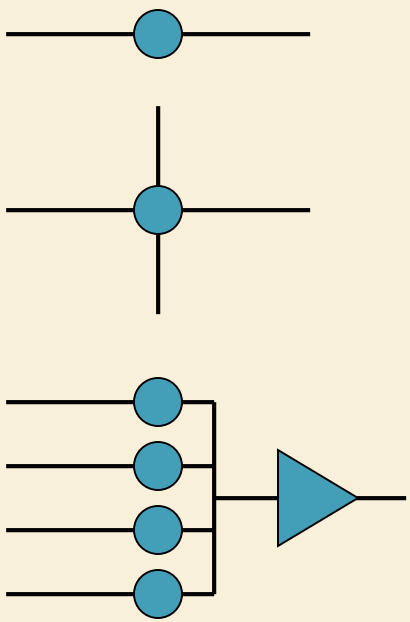
(b)

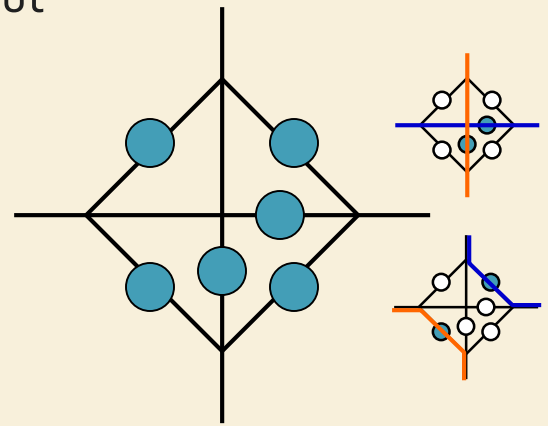


(c)

PIPs

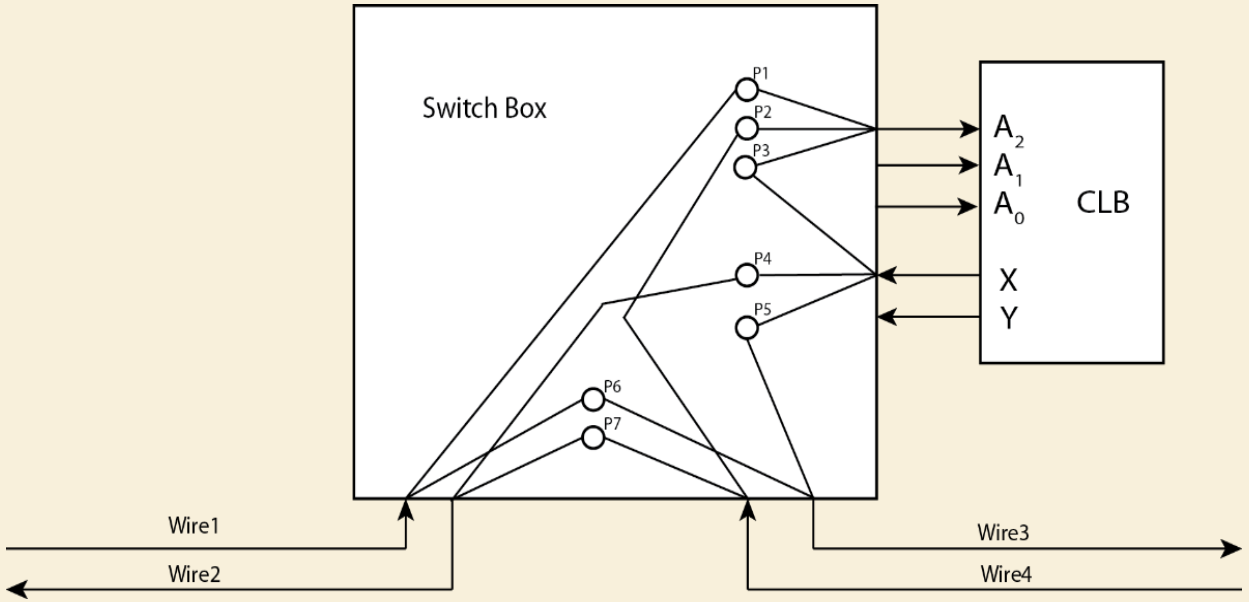
- Break-point PIP
  - Connect or isolate 2 wire segments
- Cross-point PIP
  - Turn corners
- Multiplexer PIP
  - Directional and buffered
  - Select 1-of-*N* inputs for output
    - Decoded MUX PIP – *N* config bits select from 2^N inputs
    - Non-decoded MUX PIP – 1 config bit per input
- Compound cross-point PIP
  - Collection of 6 break-point PIPs
    - Can route to two isolated signal nets





Switch box

- Connects CLB to the "routing fabric"



Spartan 3 Routing Resources

switch matrix
over 2,400 PIPs
mostly MUX PIPs

PLB consists of 4 slices

x6 wire segments

x2 wire segments

xH & xL wire segments

over 450 total wire segments in PLB

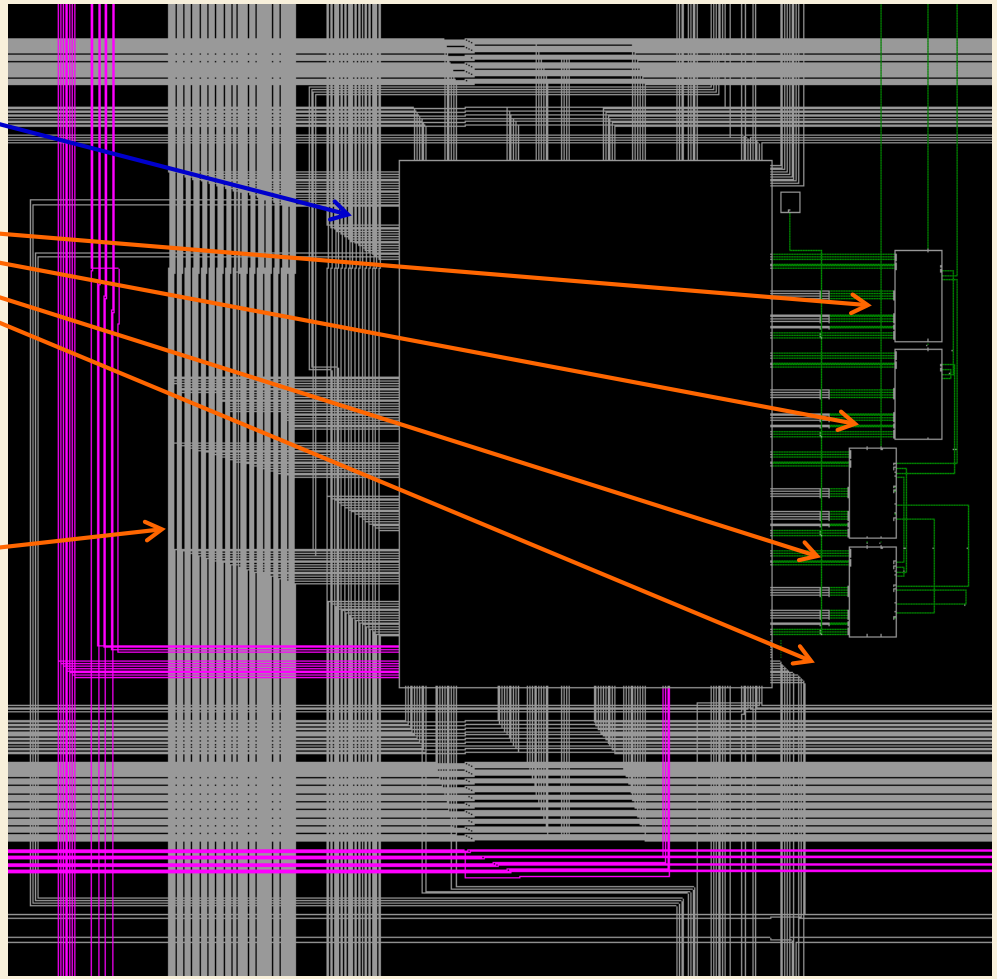


FIGURE 3-36: Direct Interconnects between Neighboring Logic Blocks

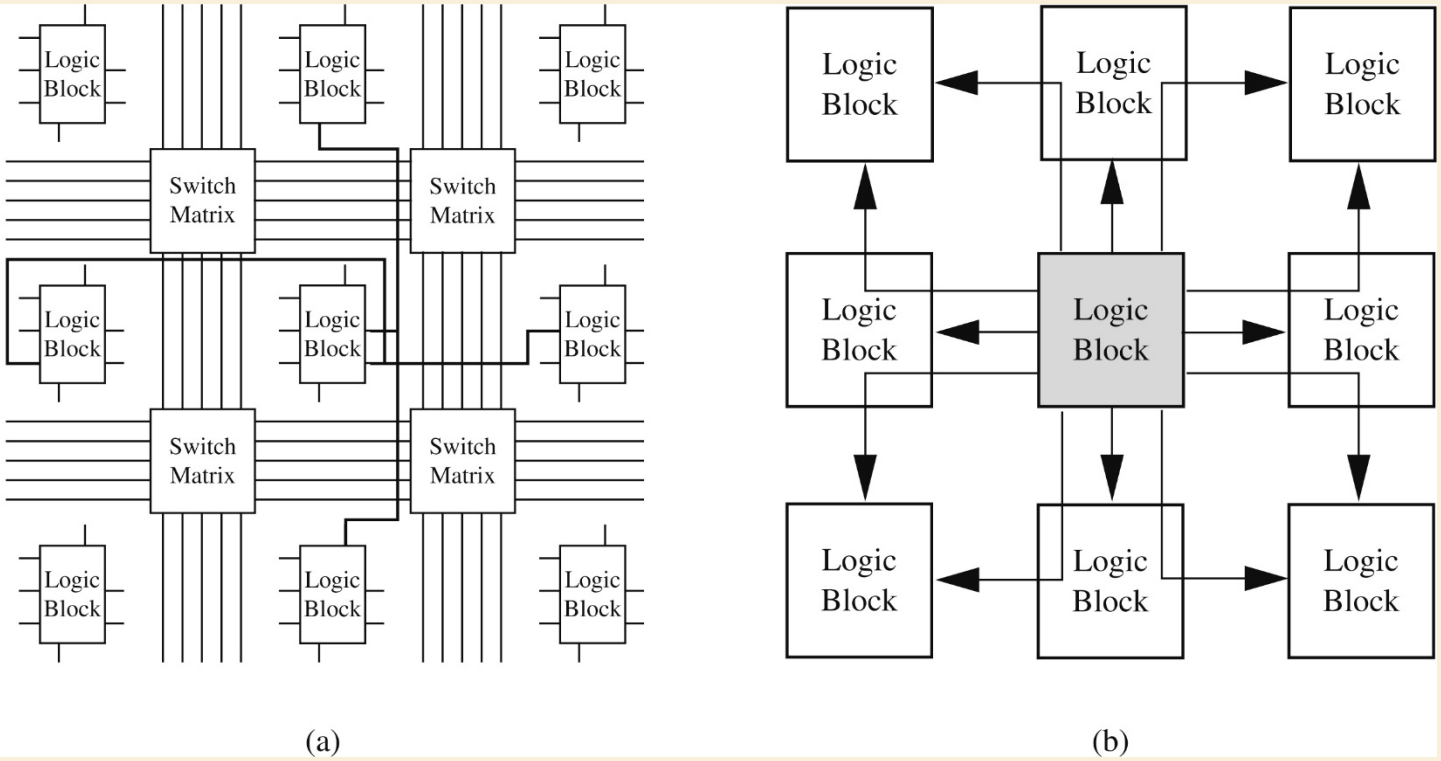
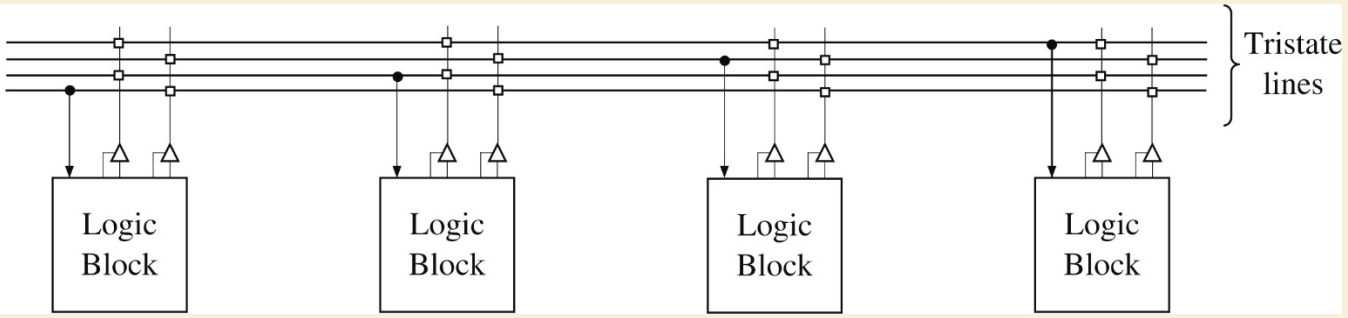
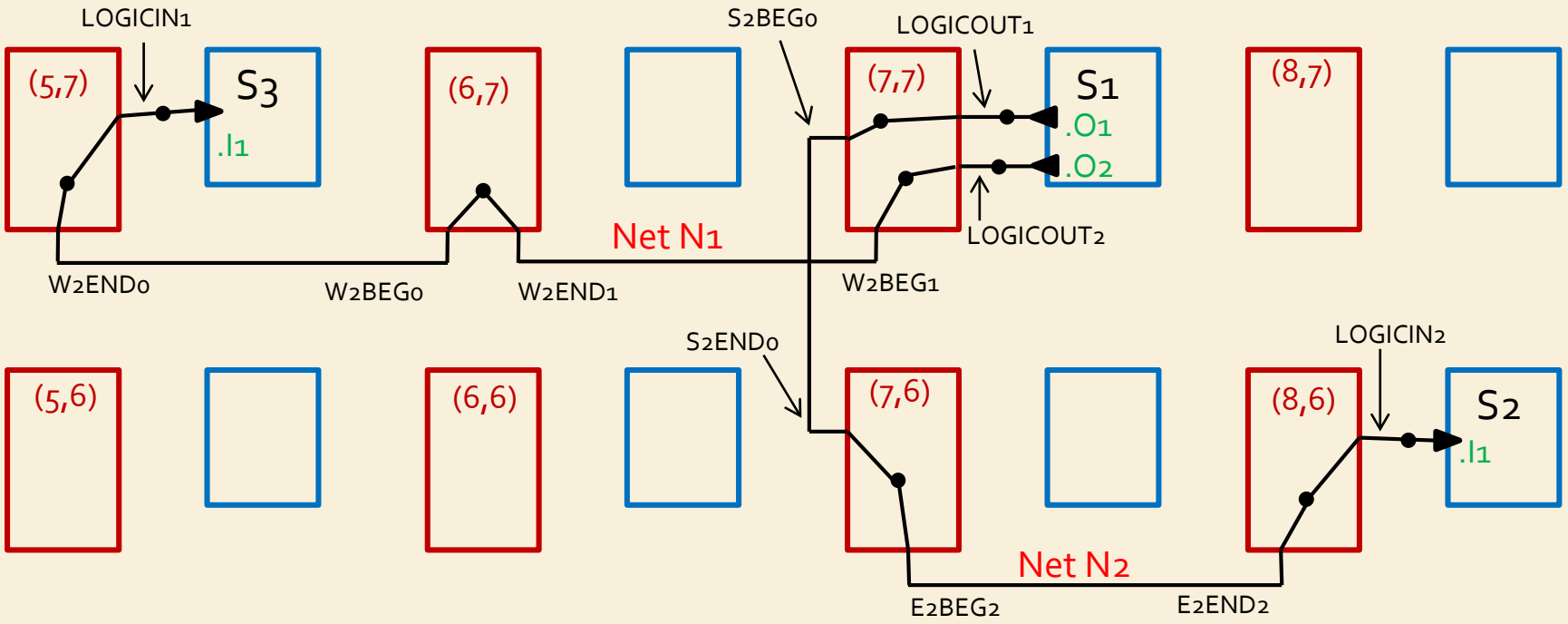


FIGURE 3-37: Global Lines



Fully routed design



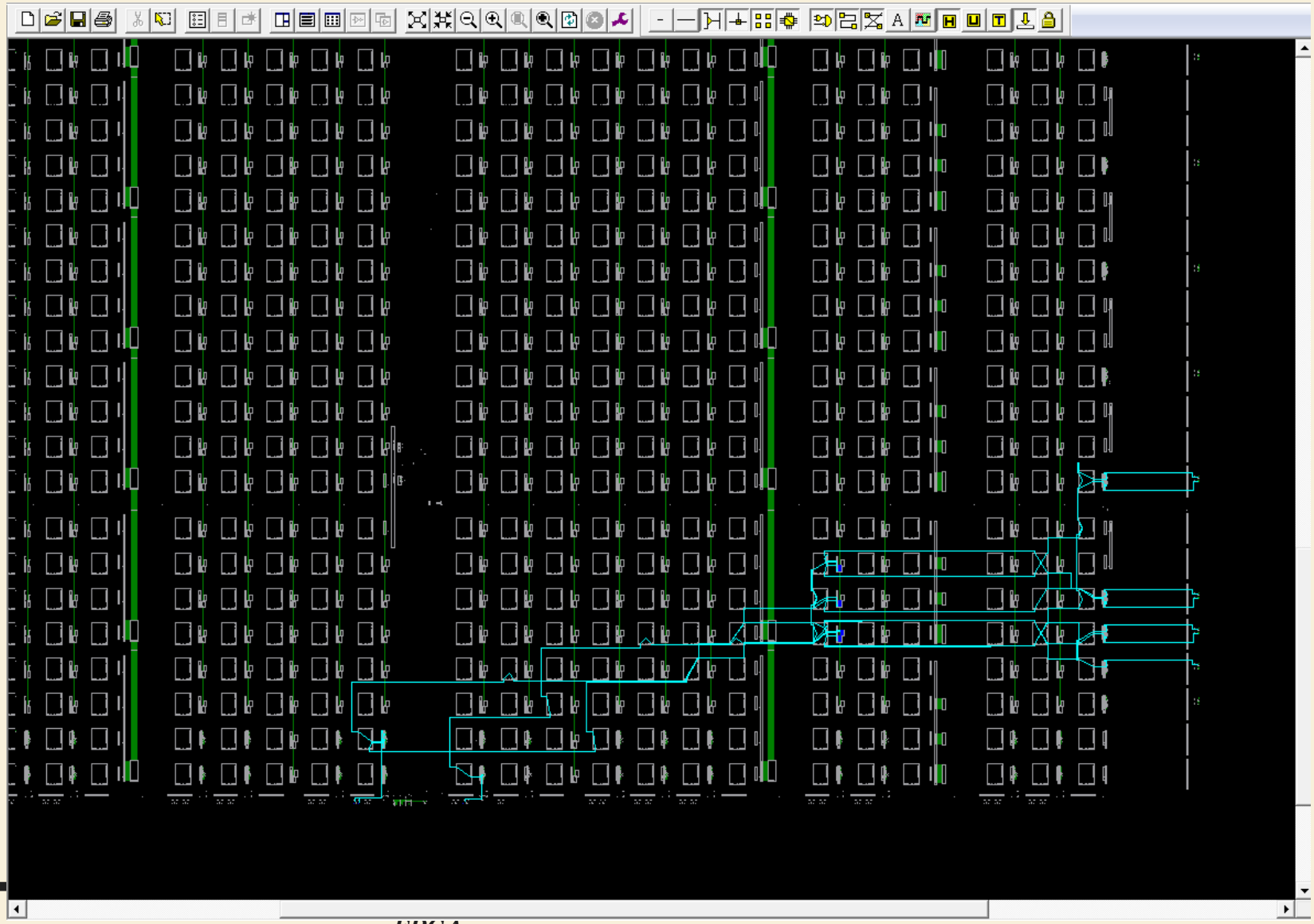
Net N1: Site S1 output pin O1 connects to input pin I1 on site S3

Net N2: Site S1 output pin O2 connects to input pin I1 on site S2

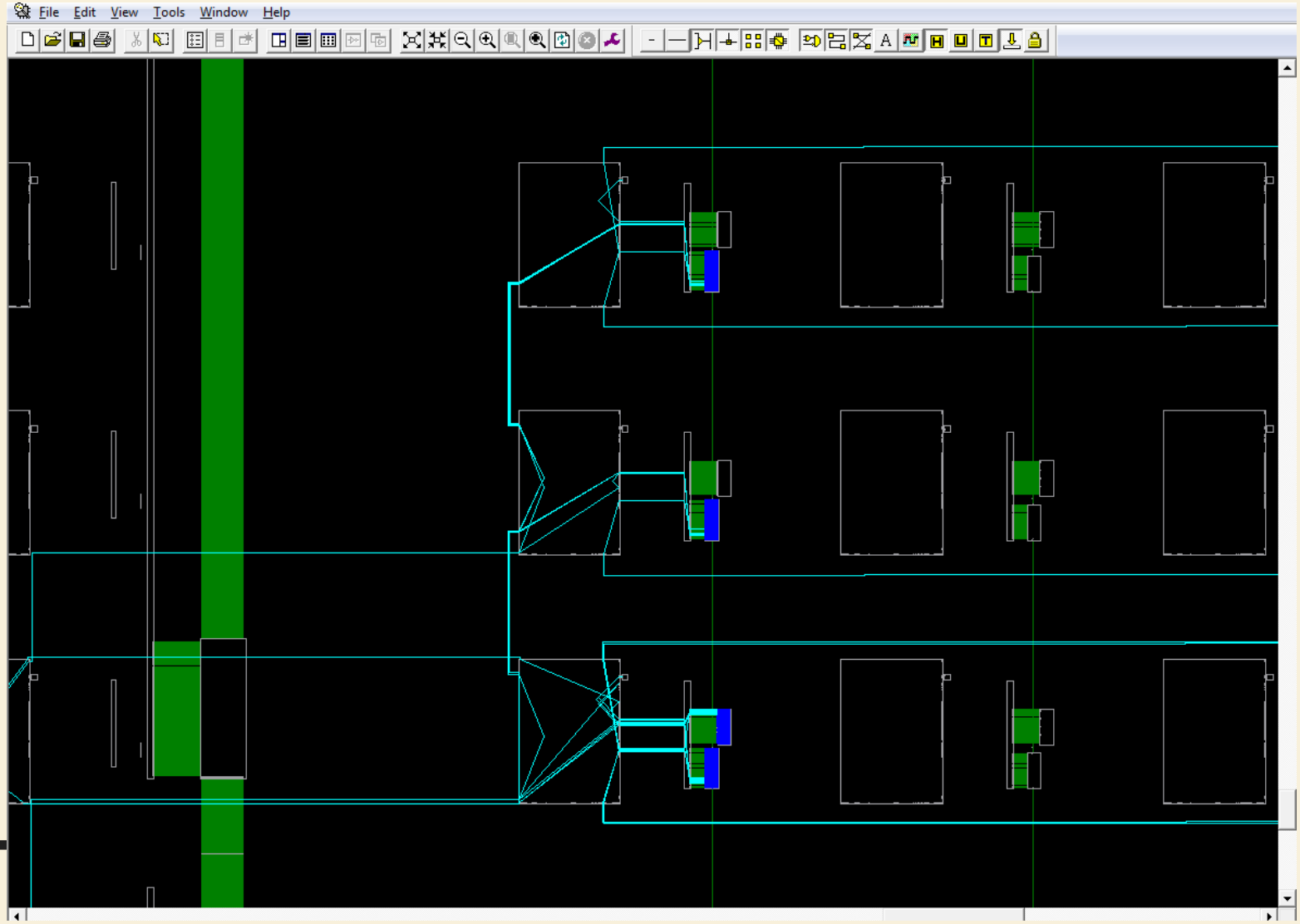
Black "dots" are routing pips

Predefined connections exist between switch boxes

ELEC 4200 Lab 0 in Spartan 6

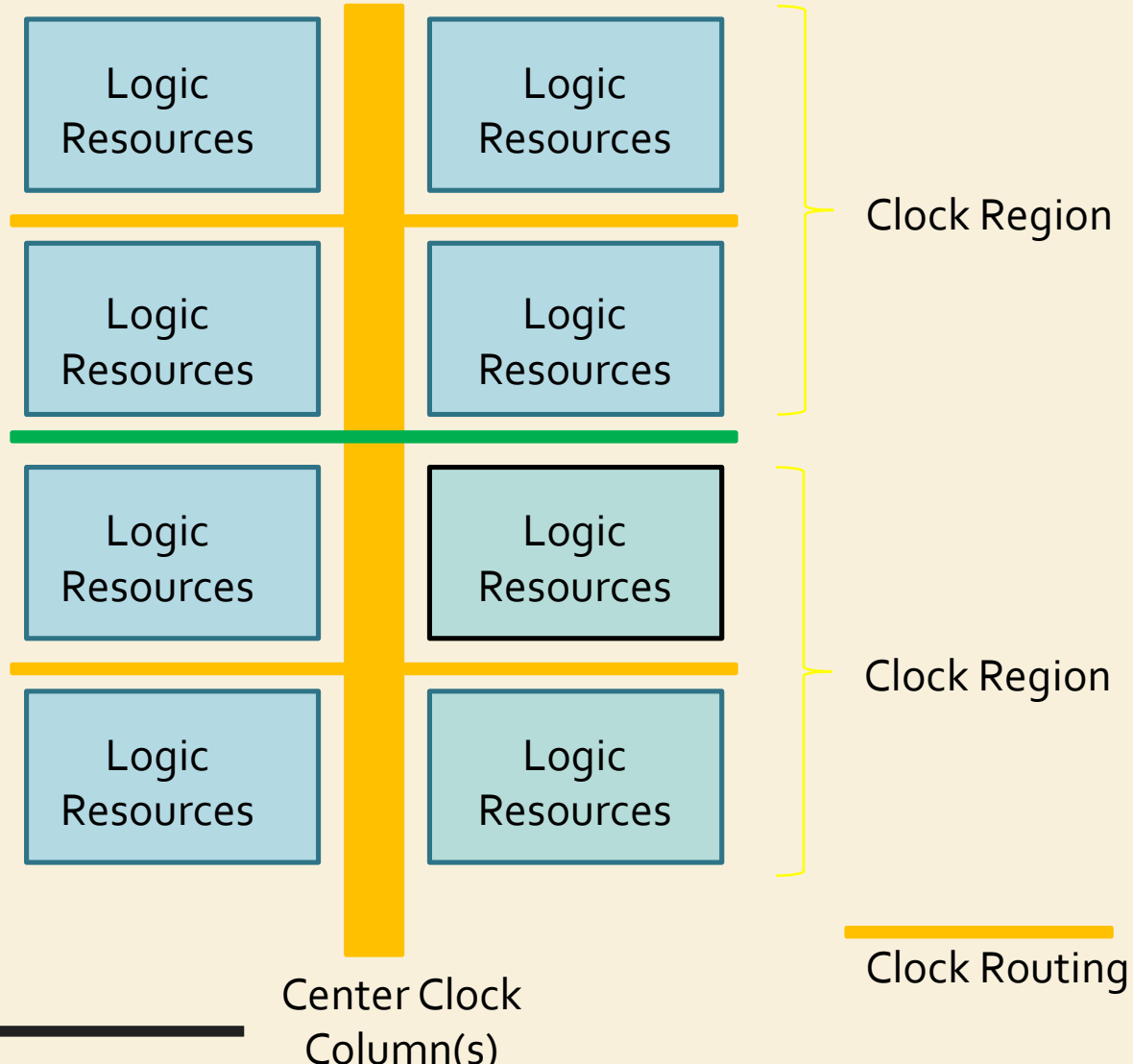


Lab 0 in Spartan 6
(routing details)

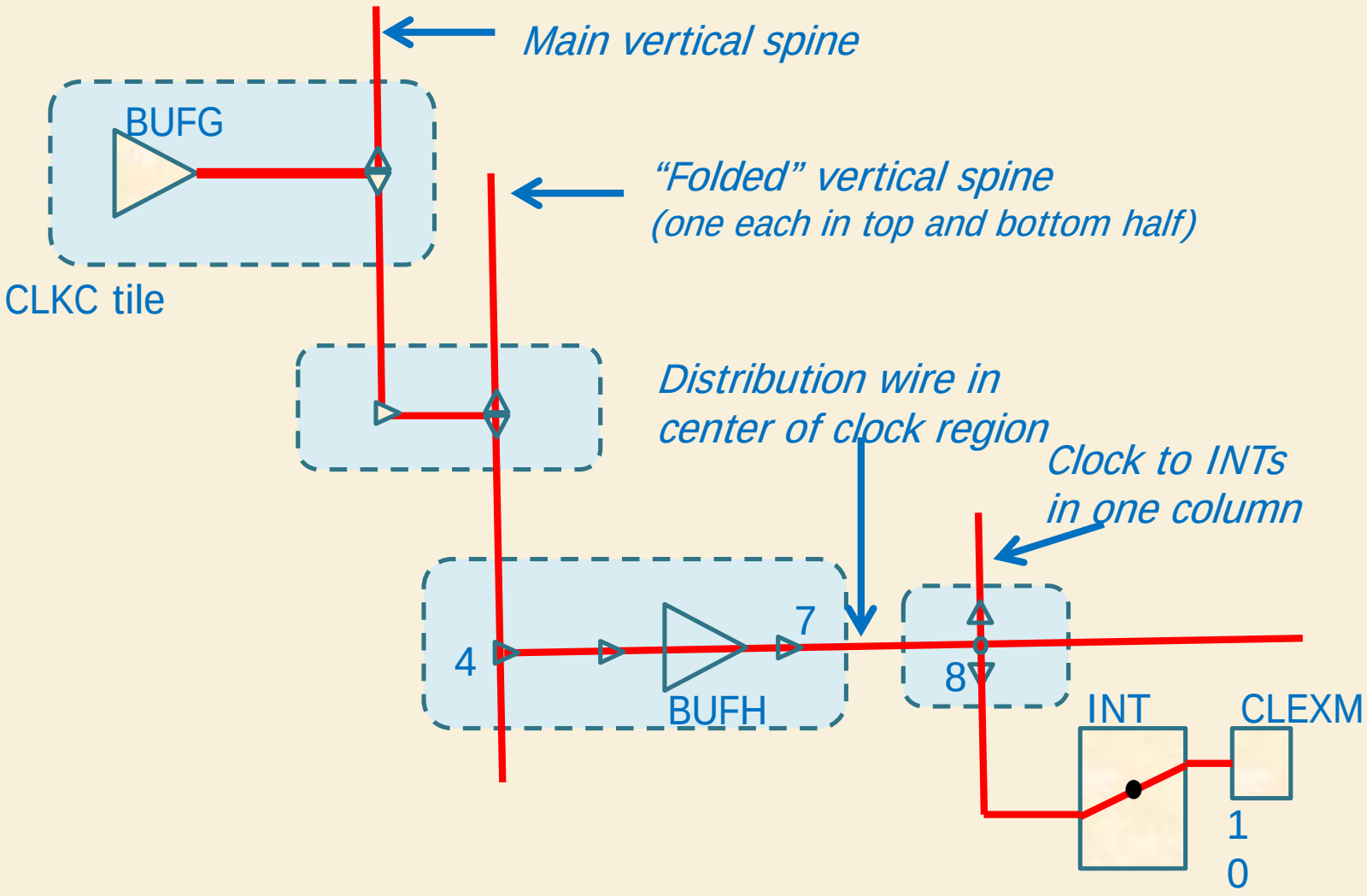


Ex: modulo7 counter (device xc6slx25t)

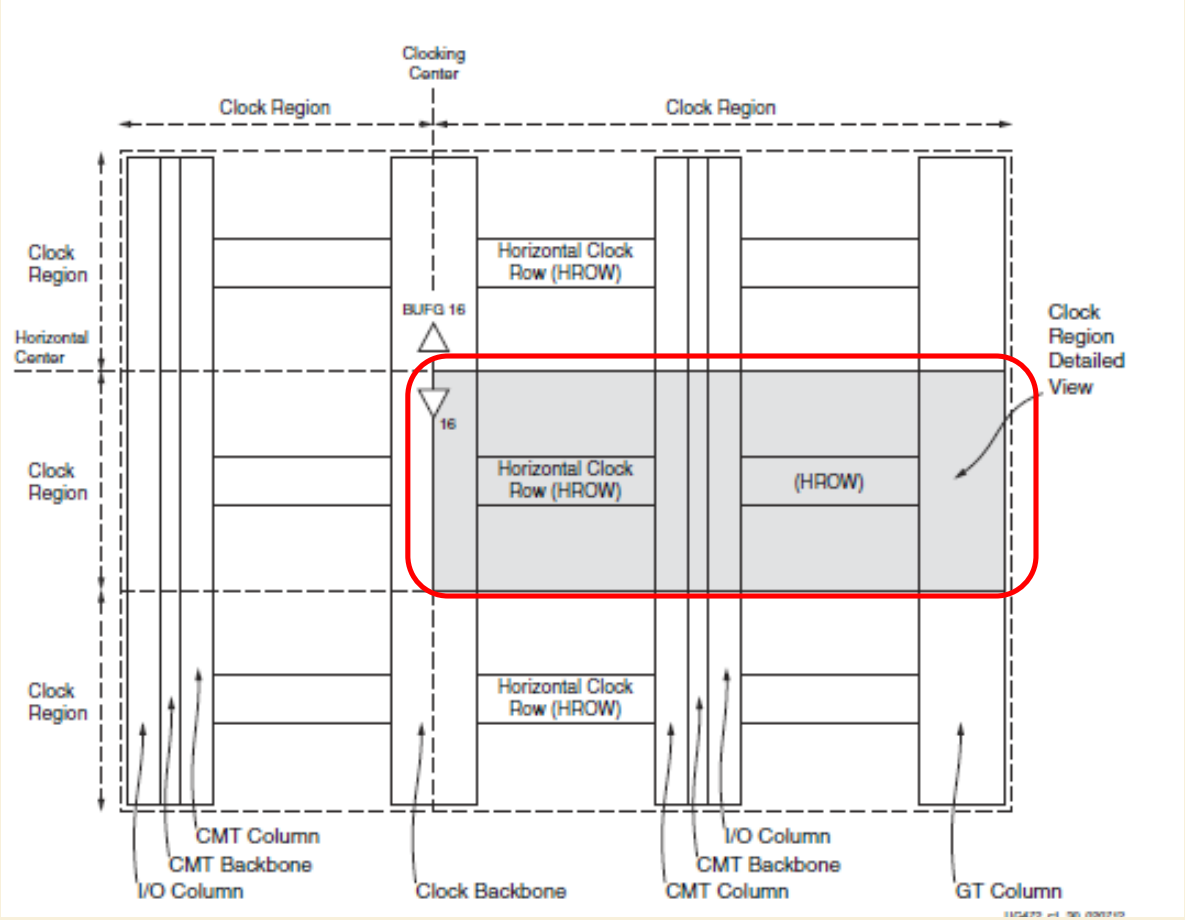
FPGA clock regions



Spartan 6 clock tree example

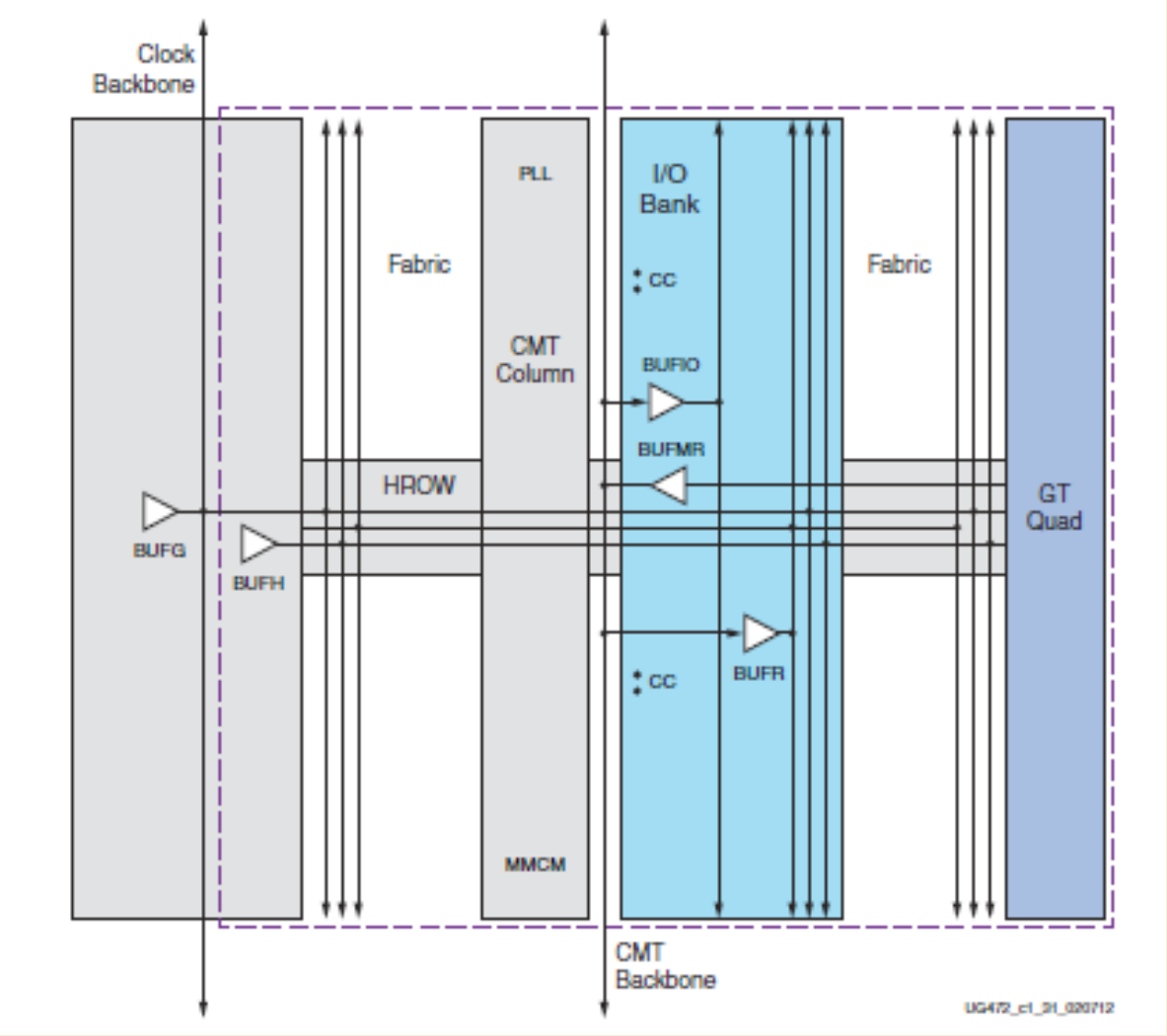


7 Series FPGA high-level clock architecture view

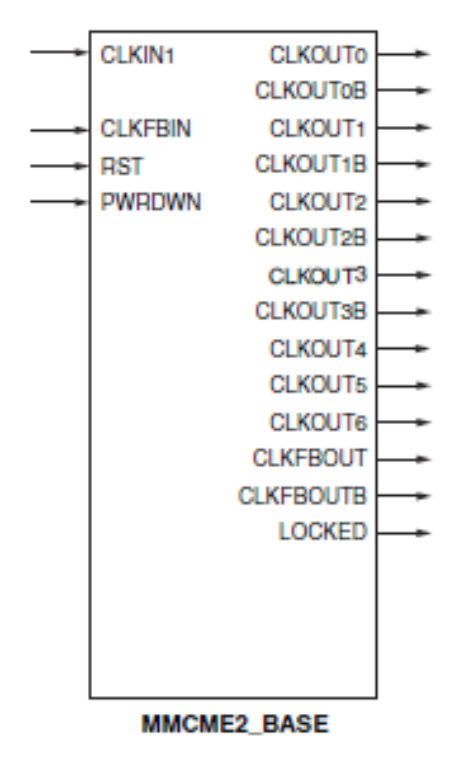


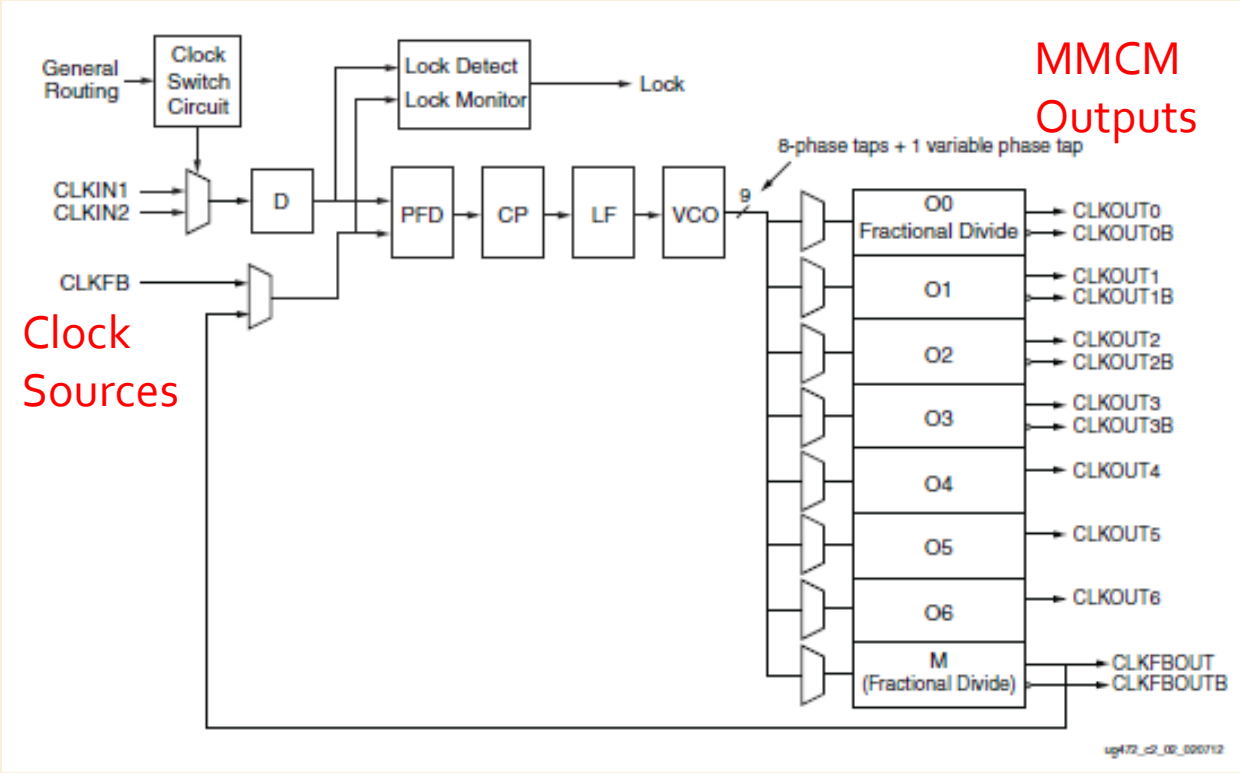
A clock region always contains 50 CLBs per column, ten 36K block RAMs per column (unless five 36K blocks are replaced by an integrated block for PCI Express®), 20 DSP slices per column, and 12 BUFHs. A clock region contains, if applicable, one CMT (PLL/MMCM), one bank of 50 I/Os, one GT quad consisting of four serial transceivers, and half a column for PCIe® in a block RAM column.

Basic view of a clock region



Clock management tile (CMT)
Mixed-mode clock manager (MMCM)

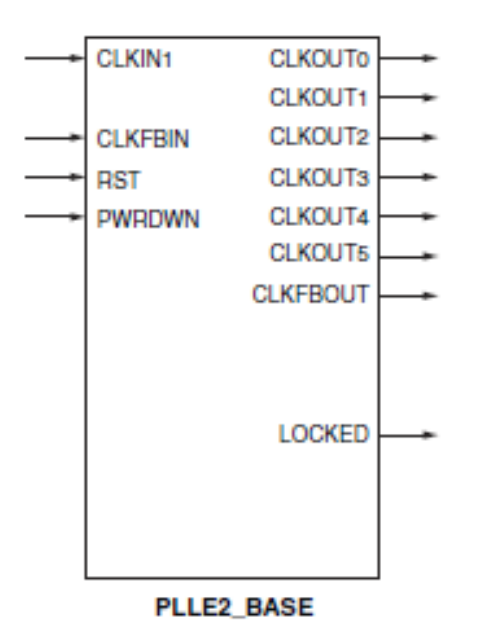


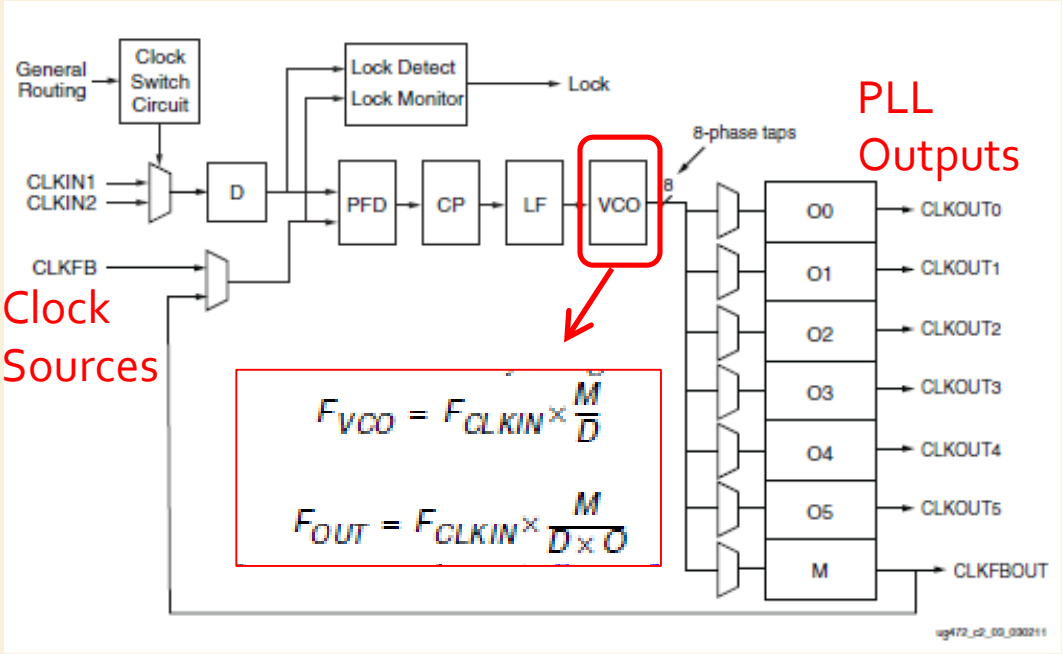


MMCM Outputs = frequency divided, phase shifted, inverted
Up to 24 CMTs per Series 7 device

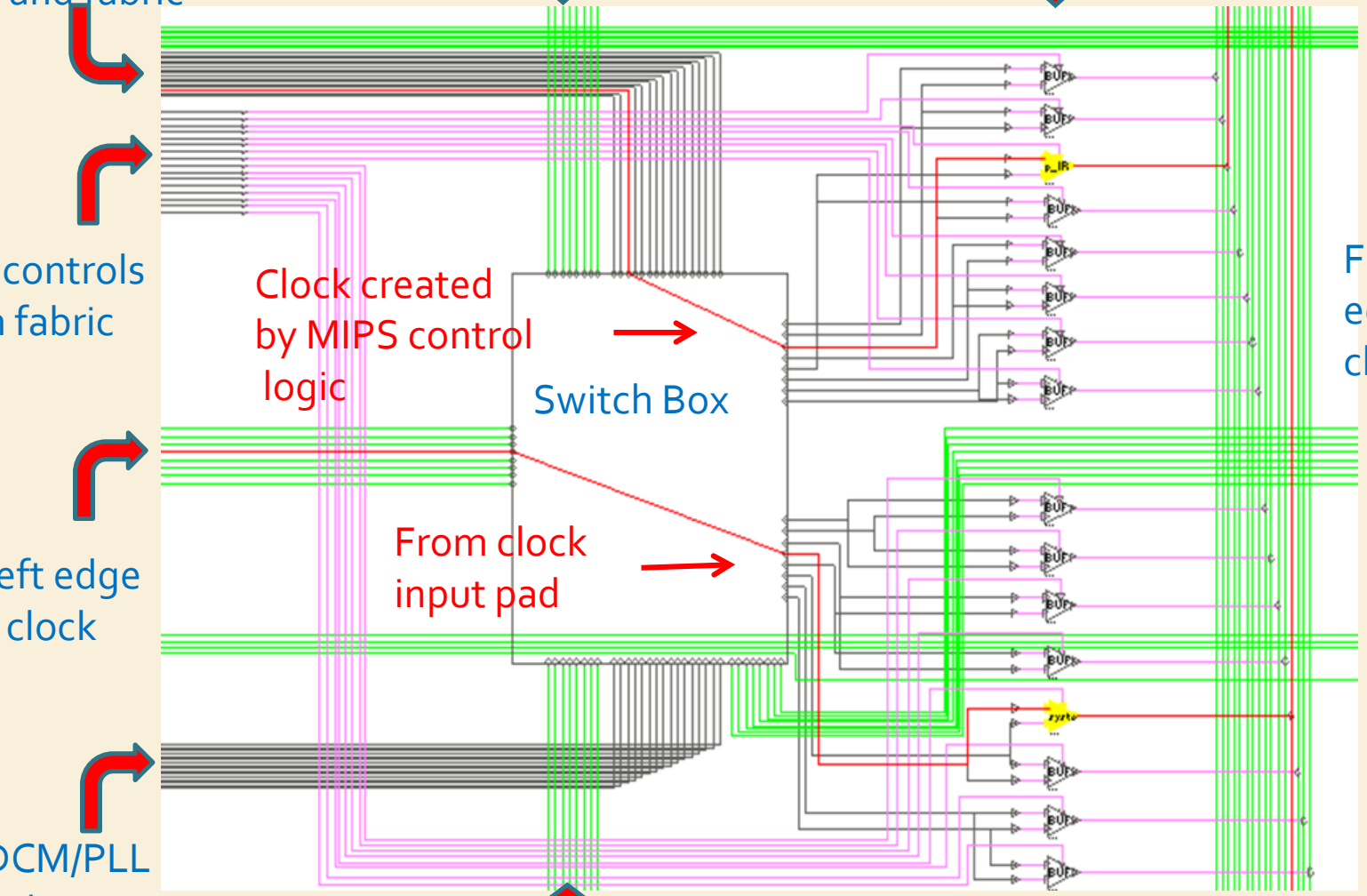
Clock management tile (CMT)
Phase-locked loop (PLL)

PLL = frequency synthesizer using a voltage-controlled oscillator (VCO)





Spartan 6 global clock sources

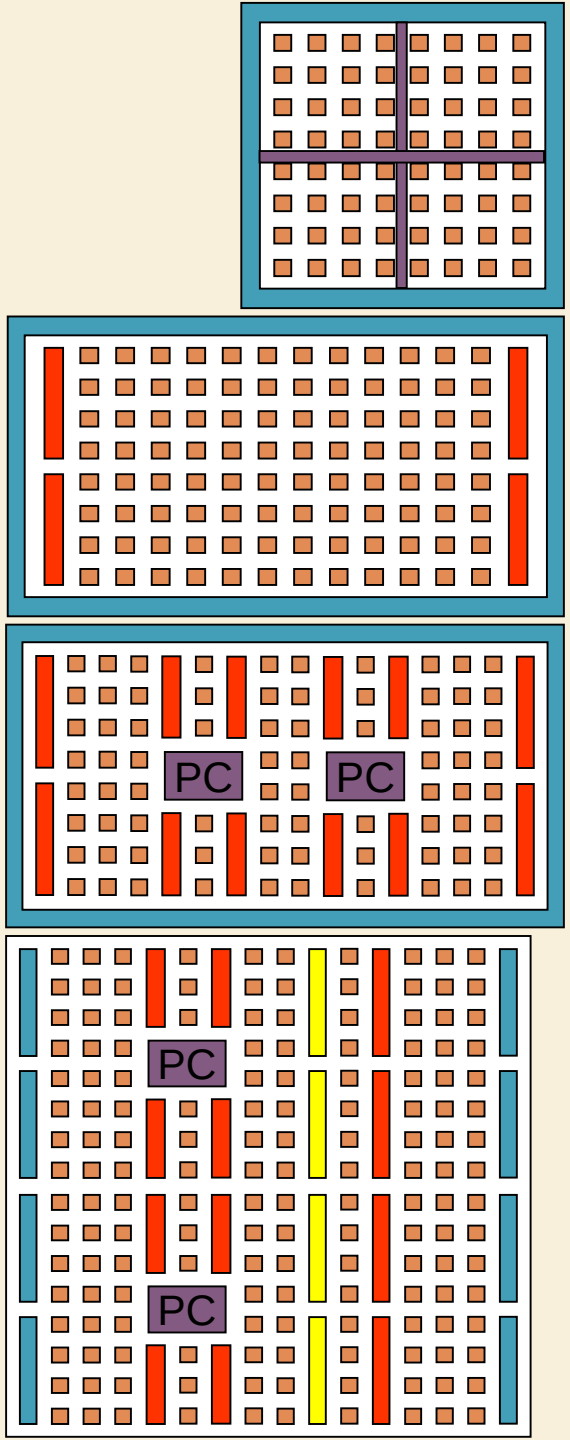


Specialized "hard " cores

- RAMs – single-port, dual-port, FIFOs
  - 128 bits to 36K bits per RAM
  - 4 to 575 RAM cores per FPGA
- DSPs – 18x18-bit multiplier, 48-bit accumulator, etc.
  - up to 512 per FPGA
- Microprocessors and/or microcontrollers
  - Up to 2 per FPGA (hard core processor)
  - Support soft core processors
    - Synthesized from HDL into programmable resources
- Communication functions
  - Gigabit transceivers
  - Ethernet MAC
  - PCE Express bus

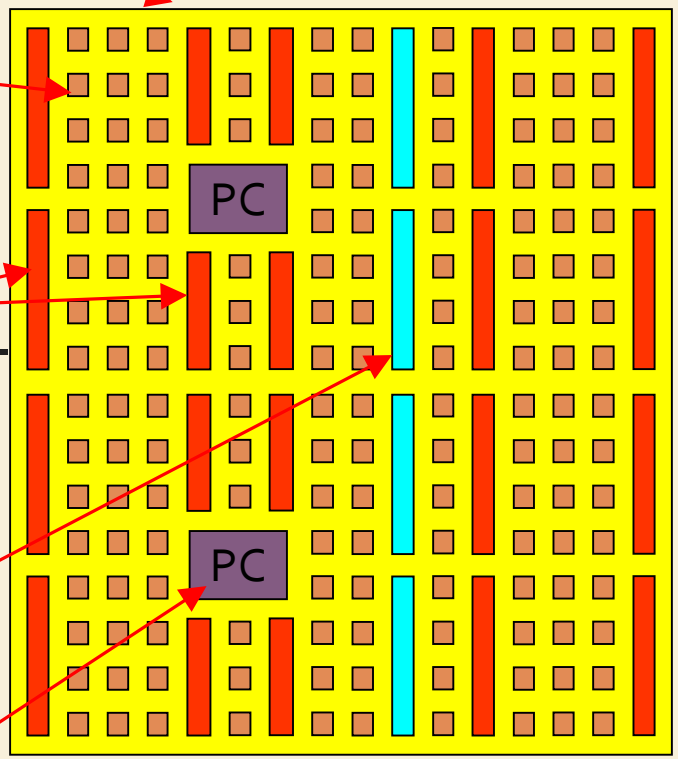
FPGA Architectures

- 4000/Spartan
  - *N*x*N* array of unit cells
    - Unit cell = CLB + routing
      - Special routing along center axes
  - I/O cells around perimeter
- Virtex/Spartan-2
  - *M*x*N* array of unit cells
  - Added block 4K RAMs at edges
- Virtex-2/Spartan-3
  - Block 18K RAMs in array
  - Added 18x18 multipliers with each RAM
  - Added PowerPCs in Virtex-2 Pro
- Virtex-4/Virtex-5
  - Added 48-bit DSP cores w/multipliers
  - I/O cells along columns for BGA



Xilinx Virtex-4 FPGAs

- Configuration memory: 4.7M to 50.8M bits of RAM
- PLBs: 1,536 to 22,272
  - 4 slices per PLB
    - 2 LUTs & 2 FFs per slice
    - 2 slices can operate as RAMs/SRs
- Block RAMs: 48 to 552 18K-bit dual-port RAMs
  - Also operate as FIFOs
- DSP cores: 32 to 512, each includes:
  - 18x18-bit multiplier
  - 48-bit adder & accumulator
- Up to 2 PowerPC processors



Block RAMs

- 36 Kbit dual-port RAM
- Each port independently configurable:
  - IK words x 36 bits
    - 32 data bits + 4 parity bits
  - 2K words x 18 bits
    - 16 data bits + 2 parity bits
  - 4K words x 9 bits
    - 8 data bits + 1 parity bit
  - 8K words x 4 bits (no parity)
  - 16K words x 2 bits (no parity)
  - 32K words x 1 bit (no parity)
- Each port has independently programmable
  - clock edge, active levels for write enable, RAM enable, reset

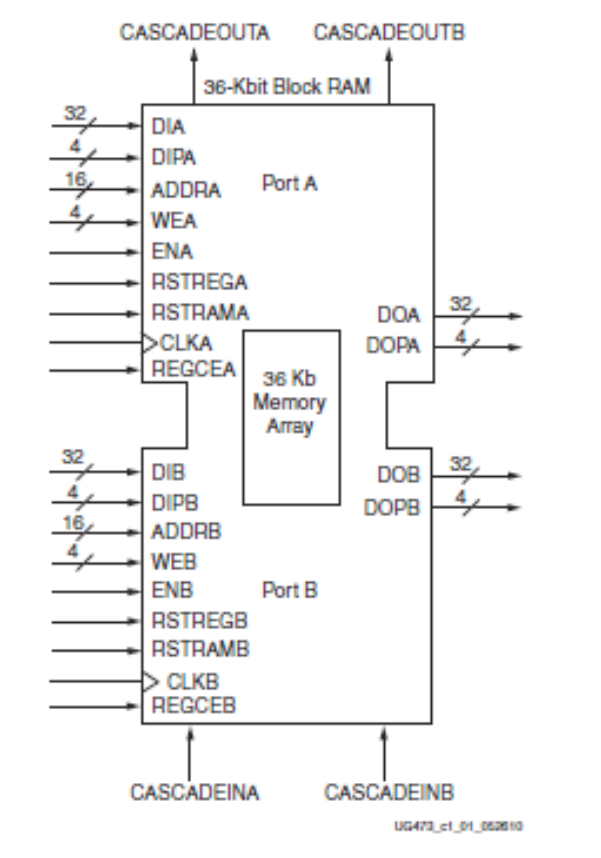


FIGURE 6-19: **Behavioral VHDL Code That Typically Infers Dedicated Memory**

```
library IEEE;
use IEEE.numeric_bit.all;

entity Memory is
  port(Address: in unsigned(6 downto 0);
       CLK, MemWrite: in bit;
       Data_In: in unsigned(31 downto 0);
       Data_Out: out unsigned(31 downto 0));
end Memory;

architecture Behavioral of Memory is
type RAM is array (0 to 127) of unsigned(31 downto 0);
signal DataMEM: RAM;  -- no initial values
begin
  process(CLK)
  begin
    if CLK'event and CLK = '1' then
      if MemWrite = '1' then
        DataMEM(to_integer(Address)) <= Data_In;  -- Synchronous Write
      end if;
      Data_Out <= DataMEM(to_integer(Address));   -- Synchronous Read
    end if;
  end process;
end Behavioral;
```

FIGURE 6-20: **Look-Up Table–Based 4 × 4 Multiplier**

```
library IEEE;
use IEEE.numeric_bit.all;

entity LUTmult is
  port(Mplier, Mcand: in unsigned(3 downto 0);
       Product: out unsigned(7 downto 0));
end LUTmult;

architecture ROM1 of LUTmult is
type ROM is array (0 to 255) of unsigned(7 downto 0);
constant PROD_ROM: ROM: =
      (x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00",
      x"00", x"01", x"02", x"03", x"04", x"05", x"06", x"07", x"08", x"09", x"0A", x"0B", x"0C", x"0D", x"0E", x"0F",
      x"00", x"02", x"04", x"06", x"08", x"0A", x"0C", x"0E", x"10", x"12", x"14", x"16", x"18", x"1A", x"1C", x"1E",
      x"00", x"03", x"06", x"09", x"0C", x"0F", x"12", x"15", x"18", x"1B", x"1E", x"21", x"24", x"27", x"2A", x"2D",
      x"00", x"04", x"08", x"0C", x"10", x"14", x"18", x"1C", x"20", x"24", x"28", x"2C", x"30", x"34", x"38", x"3C",
      x"00", x"05", x"0A", x"0F", x"14", x"19", x"1E", x"23", x"28", x"2D", x"32", x"37", x"3C", x"41", x"46", x"4B",
      x"00", x"06", x"0C", x"12", x"18", x"1E", x"24", x"2A", x"30", x"36", x"3C", x"42", x"48", x"4E", x"54", x"5A",
      x"00", x"07", x"0E", x"15", x"1C", x"23", x"2A", x"31", x"38", x"3F", x"46", x"4D", x"54", x"5B", x"62", x"69",
      x"00", x"08", x"10", x"18", x"20", x"28", x"30", x"38", x"40", x"48", x"50", x"58", x"60", x"68", x"70", x"78",
      x"00", x"09", x"12", x"1B", x"24", x"2D", x"36", x"3F", x"48", x"51", x"5A", x"63", x"6C", x"75", x"7E", x"87",
      x"00", x"0A", x"14", x"1E", x"28", x"32", x"3C", x"46", x"50", x"5A", x"64", x"6E", x"78", x"82", x"8C", x"96",
      x"00", x"0B", x"16", x"21", x"2C", x"37", x"42", x"4D", x"58", x"63", x"6E", x"79", x"84", x"8F", x"9A", x"A5",
      x"00", x"0C", x"18", x"24", x"30", x"3C", x"48", x"54", x"60", x"6C", x"78", x"84", x"90", x"9C", x"A8", x"B4",
      x"00", x"0D", x"1A", x"27", x"34", x"41", x"4E", x"5B", x"68", x"75", x"82", x"8F", x"9C", x"A9", x"B6", x"C3",
      x"00", x"0E", x"1C", x"2A", x"38", x"46", x"54", x"62", x"70", x"7E", x"8C", x"9A", x"A8", x"B6", x"C4", x"D2",
      x"00", x"0F", x"1E", x"2D", x"3C", x"4B", x"5A", x"69", x"78", x"87", x"96", x"A5", x"B4", x"C3", x"D2", x"E1");

begin
Product <= PROD_ROM(to_integer(Mplier&Mcand));  -- read Product LUT
end ROM1;
```

ROM Contents

Distributed RAM

FIGURE 6-17:
Creating Memory from LUTs

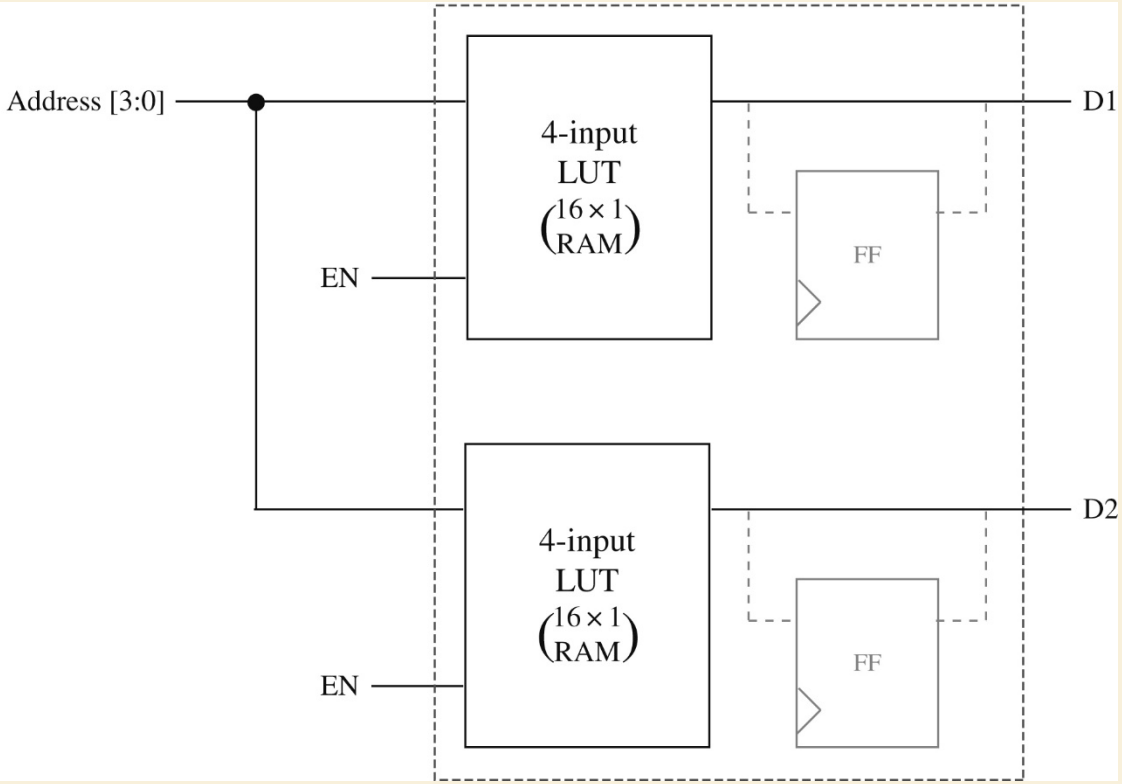


TABLE 6-2: LUT-Based RAM in Some FPGAs

FPGA Family	LUT-Based RAM (Kb)	No. of LUTs
Xilinx Virtex 5	320–3420	19200–207,360
Xilinx Virtex 4	96–987	12288–126,336
Xilinx Virtex-II	8–1456	512–93,184
Xilinx Spartan 3E	15–231*	1920–29,504
Altera Stratix II	195–2242**	12480–143,520
Altera Cyclone II	72–1069**	4608–68,416
Lattice SC	245–1884	15200–115,200
Lattice ECP2	12–136	6000–68,000

* does not use all of the LUTs as distributed RAM

** calculated from LUT counts

FIGURE 6-18: **Behavioral VHDL Code That Typically Infers LUT-Based Memory**

```
library IEEE;
use IEEE.numeric_bit.all;

entity Memory is
  port(Address: in unsigned(6 downto 0);
       CLK, MemWrite: in bit;
       Data_In: in unsigned(31 downto 0);
       Data_Out: out unsigned(31 downto 0));
end Memory;

architecture Behavioral of Memory is
type RAM is array (0 to 127) of unsigned(31 downto 0);
signal DataMEM: RAM;  -- no initial values
begin
  process(CLK)
  begin
    if CLK'event and CLK = '1' then
      if MemWrite = '1' then
        DataMEM(to_integer(Address)) <= Data_In;  -- Synchronous Write
      end if;
    end if;
  end process;

  Data_Out <= DataMEM(to_integer(Address));  -- Asynchronous Read
end Behavioral;
```

Refer to the "synthesis guide" for recommended HDL forms

DSP Blocks: Multiplier and Support Circuits

FIGURE 6-21: Dedicated Multipliers

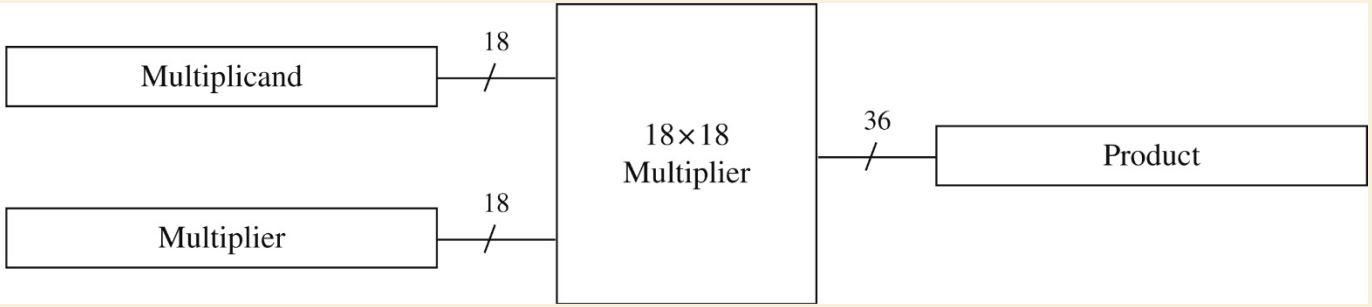
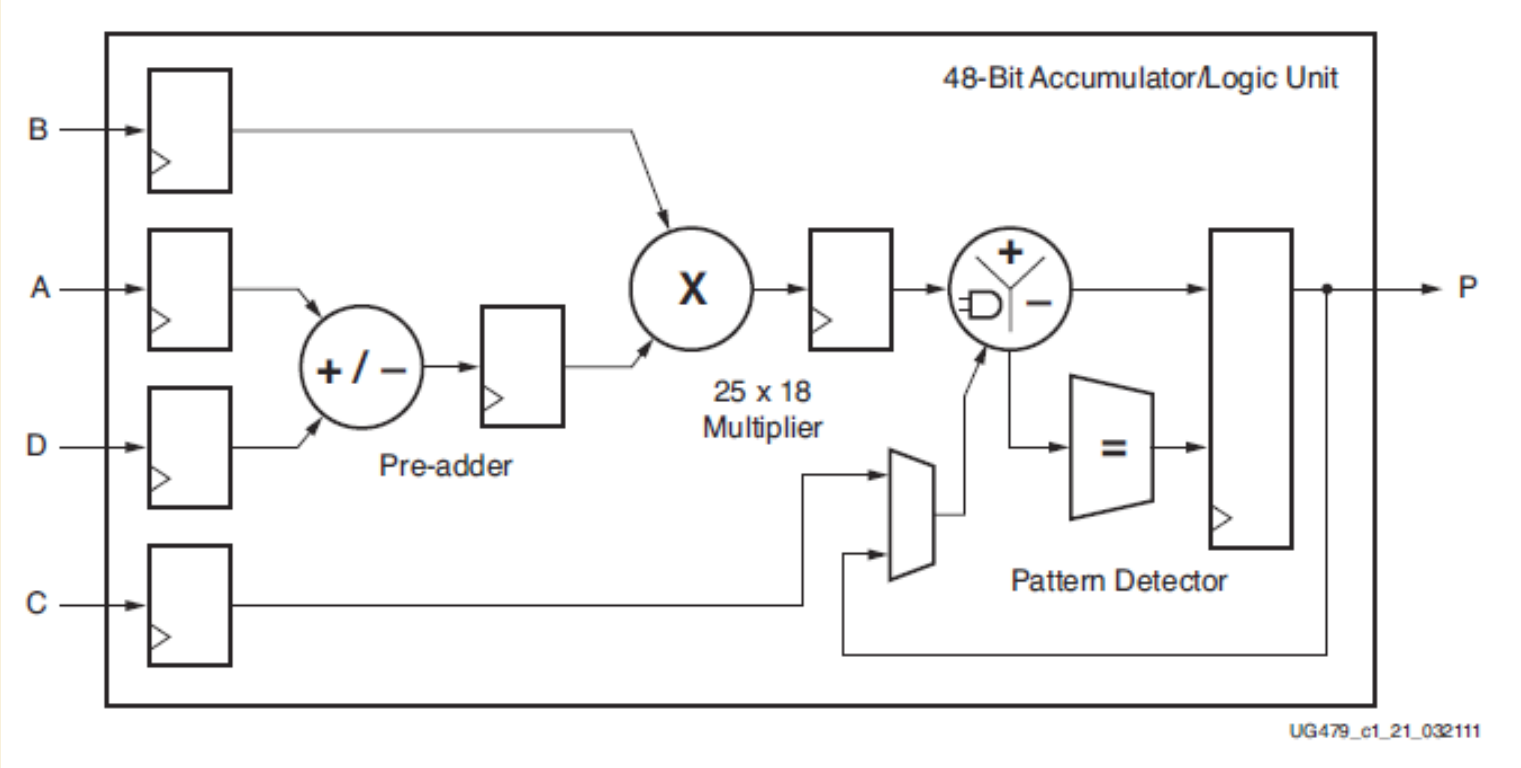


FIGURE 6-22: VHDL Code That Infers Dedicated Multipliers

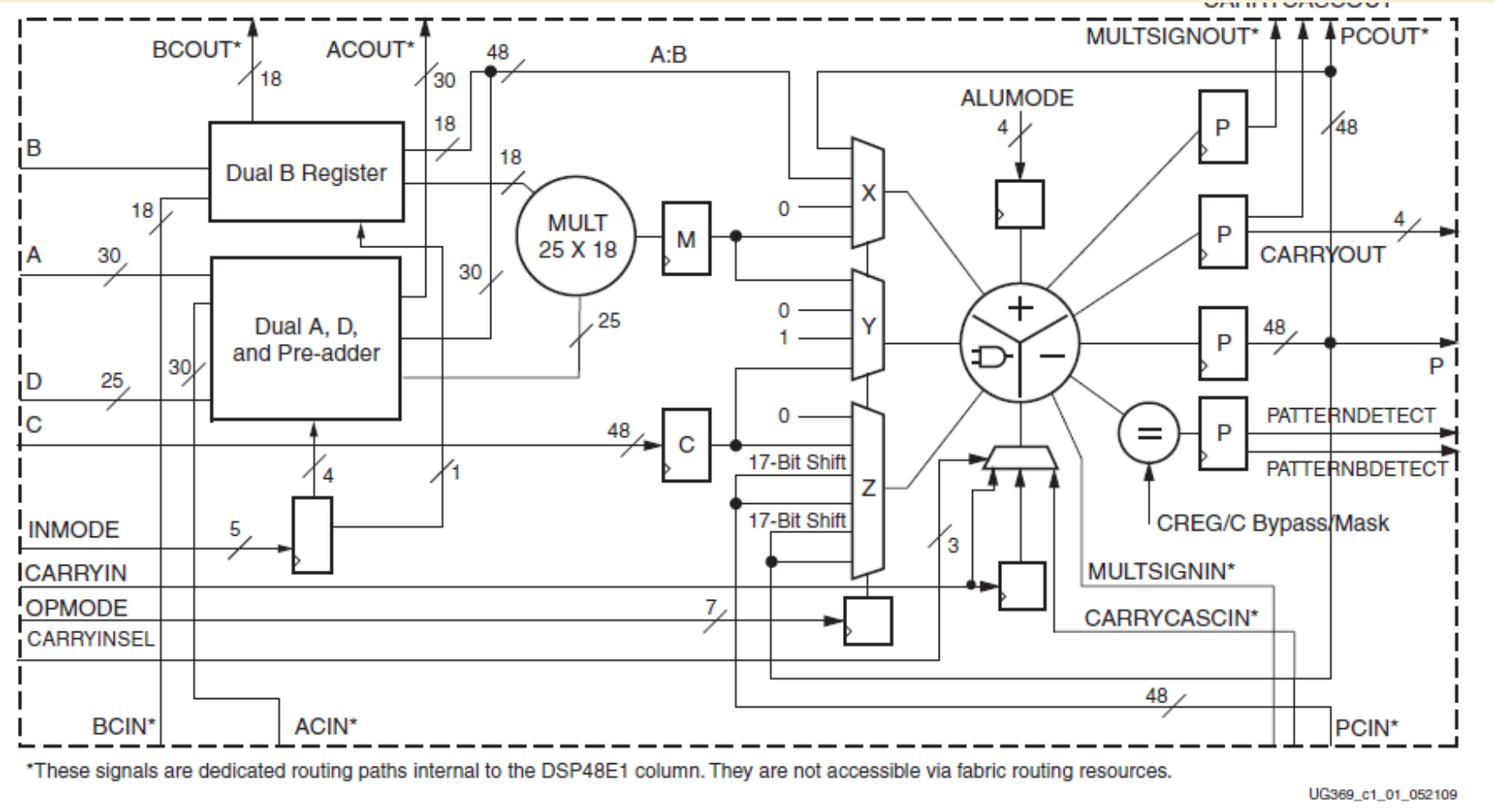
```
library IEEE;
use IEEE.numeric_bit.all;

entity multiplier is
  port(A, B: in unsigned (31 downto 0);
       C: out unsigned (63 downto 0));
end multiplier;

architecture mult of multiplier is
begin
  C <= A * B;
end mult;
```

7 Series DSP48E1 DSP slice



- 25 × 18 two's-complement multiplier: Dynamic bypass
- 48-bit accumulator: Can be used as a synchronous up/down counter
- Power-saving pre-adder: Optimizes symmetrical filter applications and reduces DSP slice requirements

DSP48E1 slice details



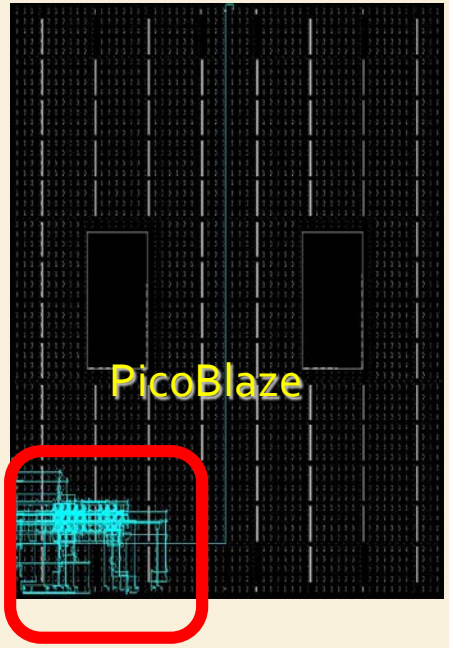
Embedded Processors

- Hard core
  - Faster
  - Fixed position
  - Few devices
- Soft core
  - Slower
  - Can be placed anywhere
  - Applicable to many devices

- Virtex-4 Processors:

ARM Processors in 7 Series

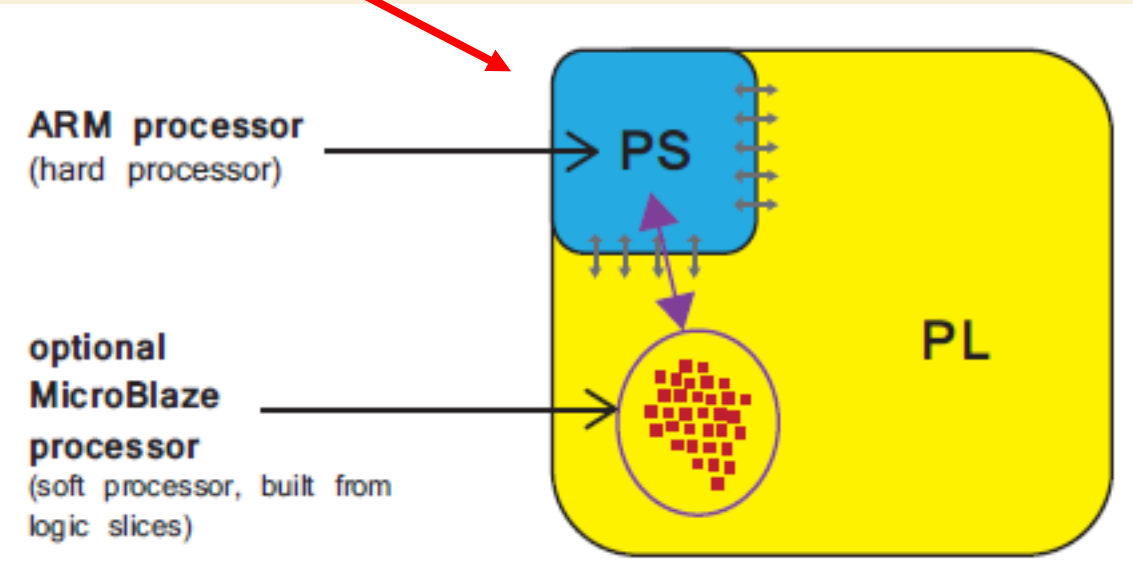
Embedded Processor	Core Type	Max Clock Frequency	Slices	PLBs	Block RAMs
PowerPC	Hard	222 MHz	1000	250	9
Microblaze	Soft	180 MHz	940	235	9
Picoblaze	Soft	221 MHz	333	84	3
Picoblaze (optimized)	Soft	233 MHz	274	69	3



Xilinx Zynq SoC devices

Zynq-7000 SoC: Dual-core ARM Cortex-A9 MPCore (up to 1GHz)
Zynq UltraScale+ MPSoC:

- Quad-core ARM Cortex-A53 MP (up to 1.5 GHz)
- Dual-core ARM Cortex-R5 MPCore (up to 600MHz)
- GPY ARM Mali-400 MP2 (up to 667MHz)



PL = Programmable Logic

Zynq-7000 SoC Features (1)

Processing System Resources

Zynq-7000 All Programmable SoC								
	Device Name	**Z-7010**	**Z-7015**	**Z-7020**	**Z-7030**	**Z-7035**	**Z-7045**	**Z-7100**
	Part Number	**XC7Z010**	**XC7Z015**	**XC7Z020**	**XC7Z030**	**XC7Z035**	**XC7Z045**	**XC7Z100**
Processing System	Processor Core	Dual-core ARM® Cortex™-A9 MPCore™ with CoreSight™						
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
	Maximum Frequency	667 MHz (-1); 766 MHz (-2); 866 MHz (-3)			667 MHz (-1); 800 MHz (-2); 1 GHz (-3)			667 MHz (-1) 800 MHz (-2)
	L1 Cache	32 KB Instruction, 32 KB data per processor						
	L2 Cache	512 KB						
	On-Chip Memory	256 KB						
	External Memory Support[1]	DDR3, DDR3L, DDR2, LPDDR2						
	External Static Memory Support[1]	2x Quad-SPI, NAND, NOR						
	DMA Channels	8 (4 dedicated to Programmable Logic)						
	Peripherals[1]	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Peripherals w/ built-in DMA[1]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
	Security[2]	RSA Authentication, and AES and SHA 256-bit Decryption and Authentication for Secure Boot						
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)		2x AXI 32b Master 2x AXI 32-bit Slave 4x AXI 64-bit/32-bit Memory AXI 64-bit ACP 16 Interrupts						

Continued next slide

Zynq-7000 SoC Features (2)

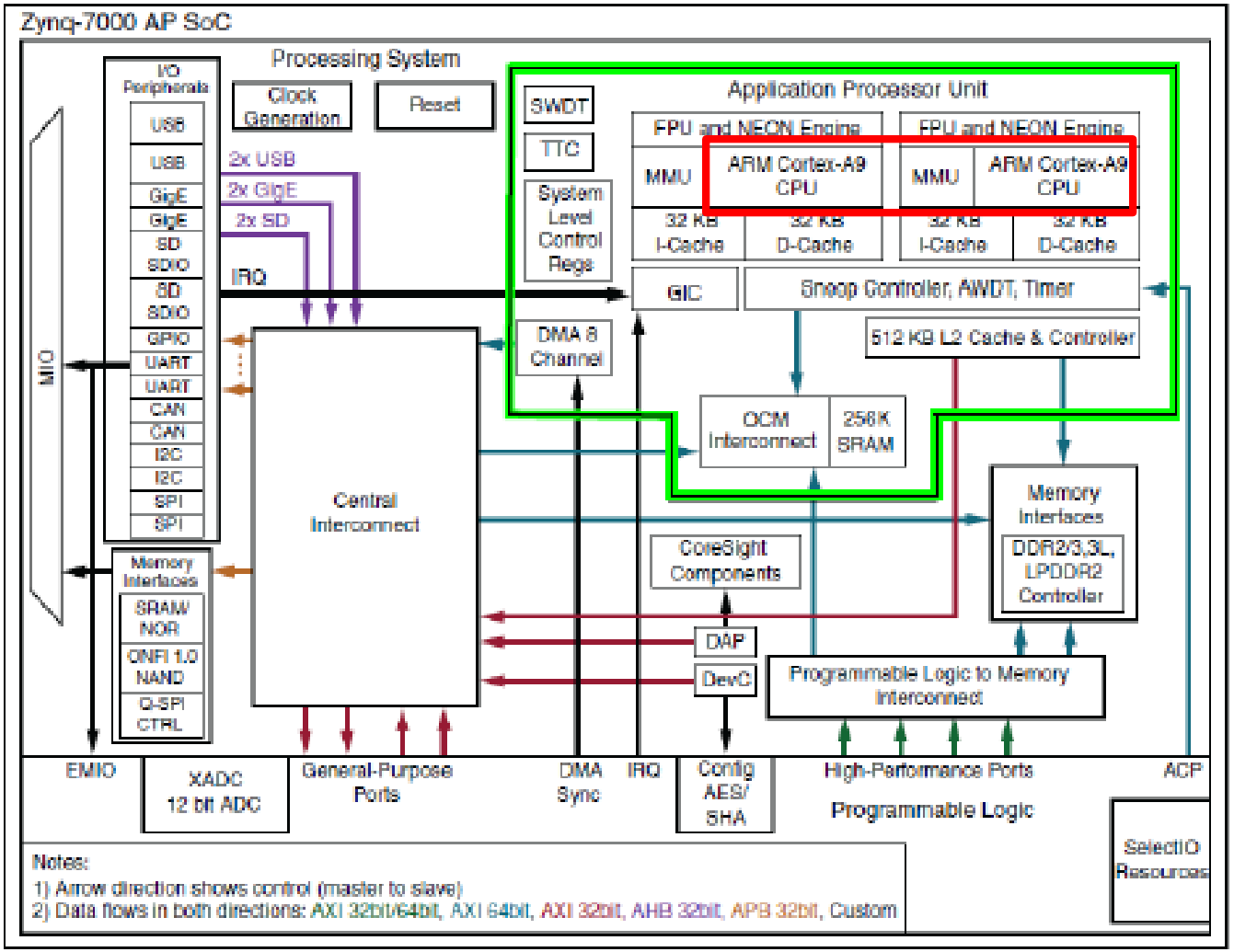
Programmable Logic Resources

Zynq-7000 All Programmable SoC								
	Device Name	**Z-7010**	**Z-7015**	**Z-7020**	**Z-7030**	**Z-7035**	**Z-7045**	**Z-7100**
	Part Number	**XC7Z010**	**XC7Z015**	**XC7Z020**	**XC7Z030**	**XC7Z035**	**XC7Z045**	**XC7Z100**
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(3)	28K Logic Cells (~430K)	74K Logic Cells (~1.1M)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	275K Logic Cells (~4.1M)	350K Logic Cells (~5.2M)	444K Logic Cells (~6.6M)
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	390 KB (95)	560 KB (140)	1,060 KB (265)	2,000 KB (500)	2,180 KB (545)	3,020 KB (755)
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACs	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)(4)	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs						
	Security(2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication						

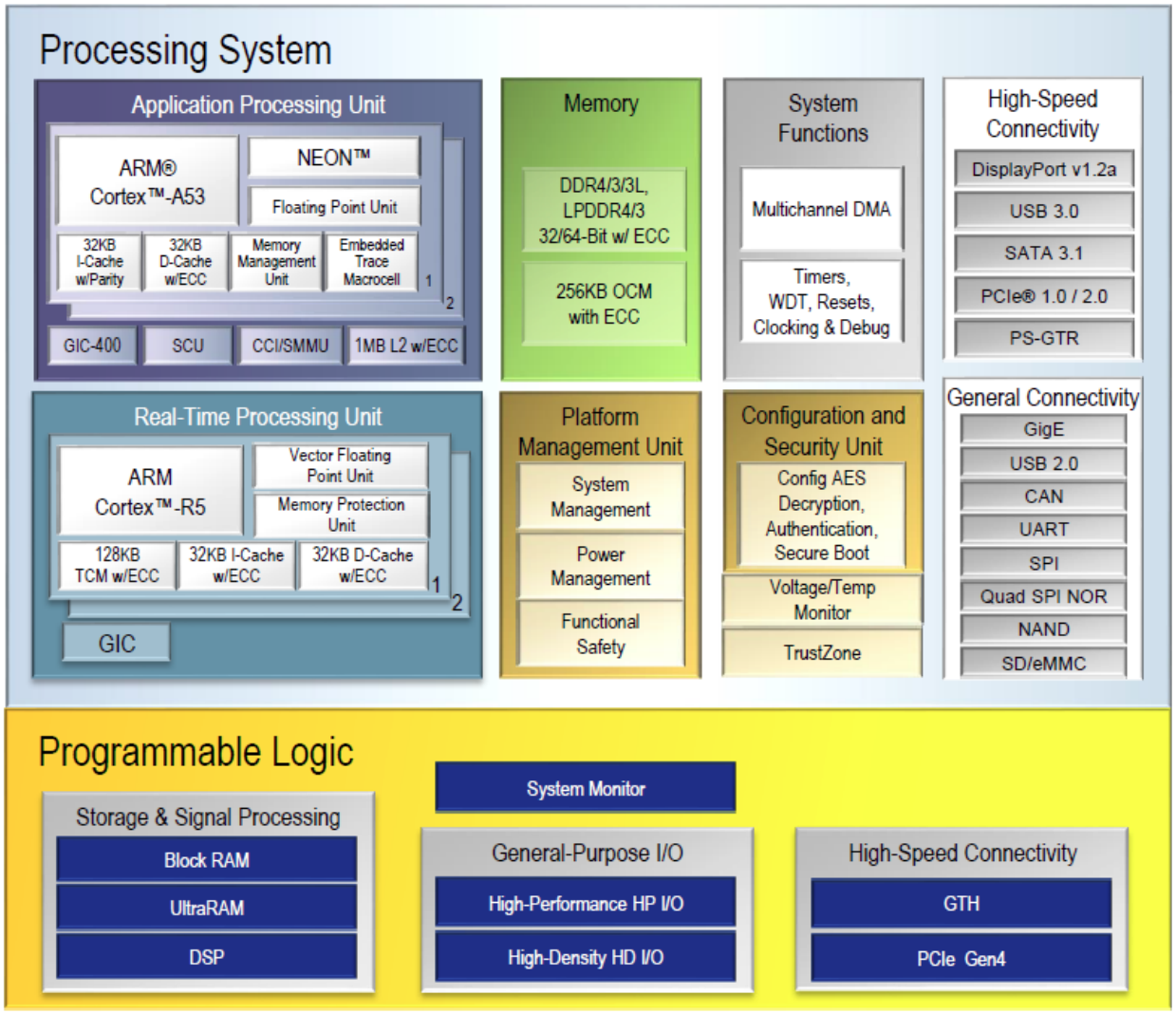
Zynq® UltraScale+™ MPSoCs

	CG Devices	EG Devices	EV Devices
Application Processor	**Dual**-core ARM® Cortex™-A53 MPCore™ up to **1.3GHz**	**Quad**-core ARM Cortex-A53 MPCore up to **1.5GHz**	**Quad**-core ARM Cortex-A53 MPCore up to **1.5GHz**
Real-Time Processor	Dual-core ARM Cortex-R5 MPCore up to **533MHz**	Dual-core ARM Cortex-R5 MPCore up to **600MHz**	Dual-core ARM Cortex-R5 MPCore up to **600MHz**
Graphics Processor		Mali™-400 MP2	Mali™-400 MP2
Video Codec			H.264 / H.265
Programmable Logic	103K–600K System Logic Cells	103K–1143K System Logic Cells	192K–504K System Logic Cells
Applications	• Sensor Processing & Fusion • Motor Control • Low-cost Ultrasound • Traffic Engineering	• Flight Navigation • Missile & Munitions • Military Construction • Secure Solutions • Networking • Cloud Computing Security • Data Center • Machine Vision • Medical Endoscopy	• Situational Awareness • Surveillance/Reconnaissance • Smart Vision • Image Manipulation • Graphic Overlay • Human Machine Interface • Automotive ADAS • Video Processing • Interactive Display

Zynq-7000 SoC Processor System

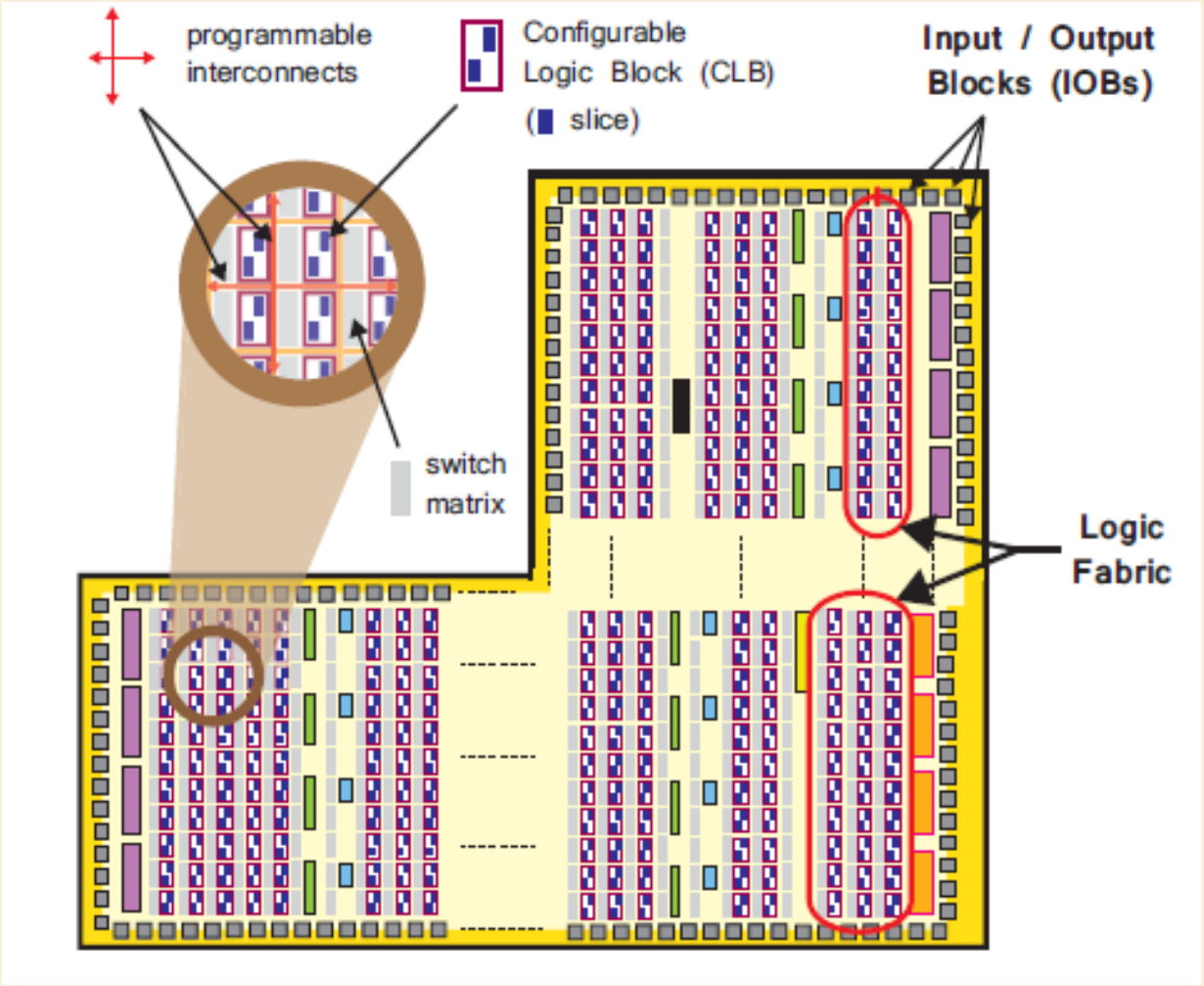


Zynq® UltraScale+™ MPSoCs: CG Block Diagram



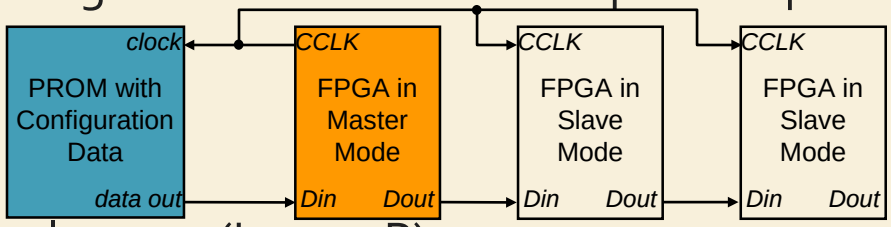
Zynq-7000 SoC Logic Fabric

Series-7 CLBs, IOBs, etc. (as in Artix-7)



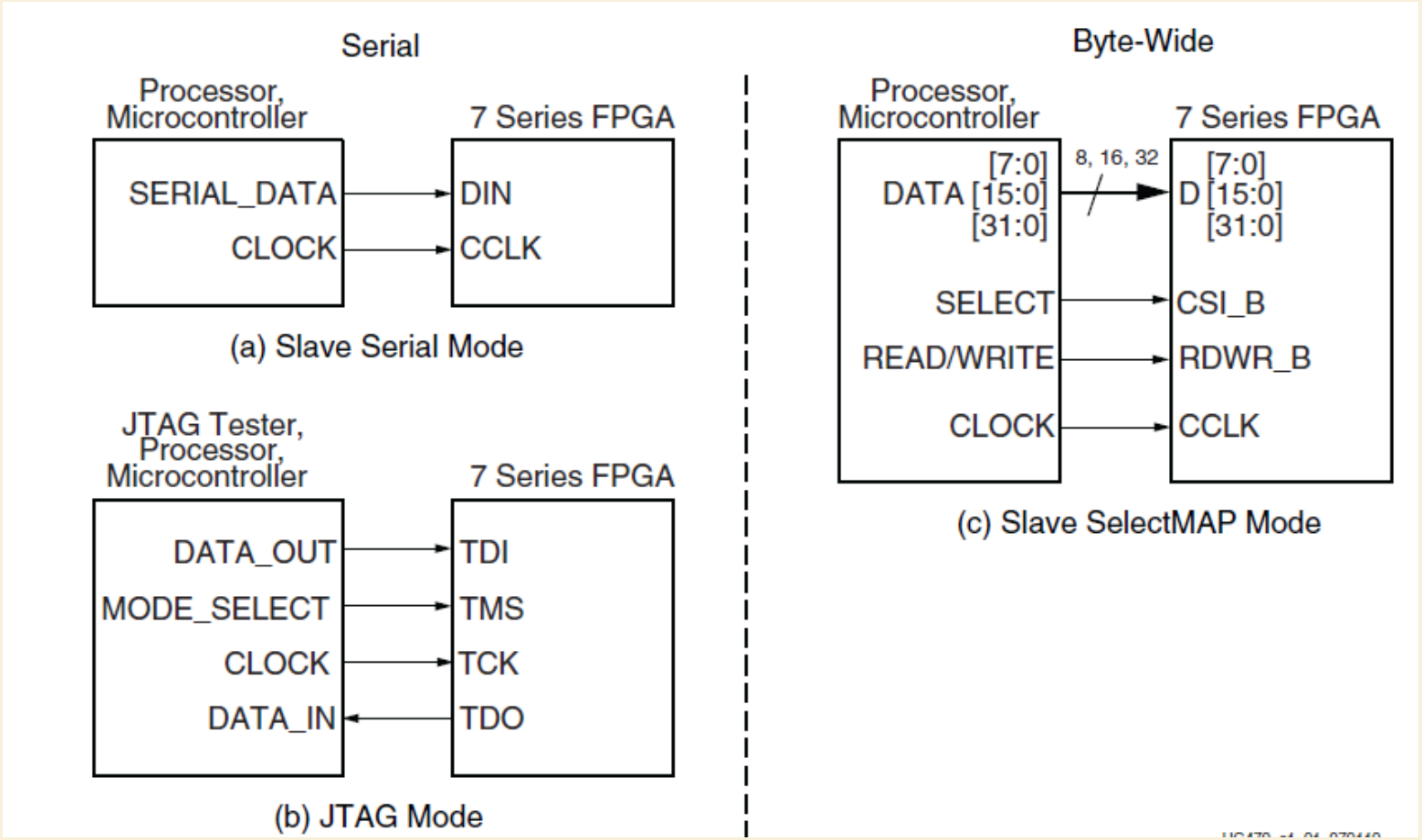
Configuration Interfaces

- Master – FPGA retrieves its own configuration from ROM after power-up
  - Serial or Parallel options



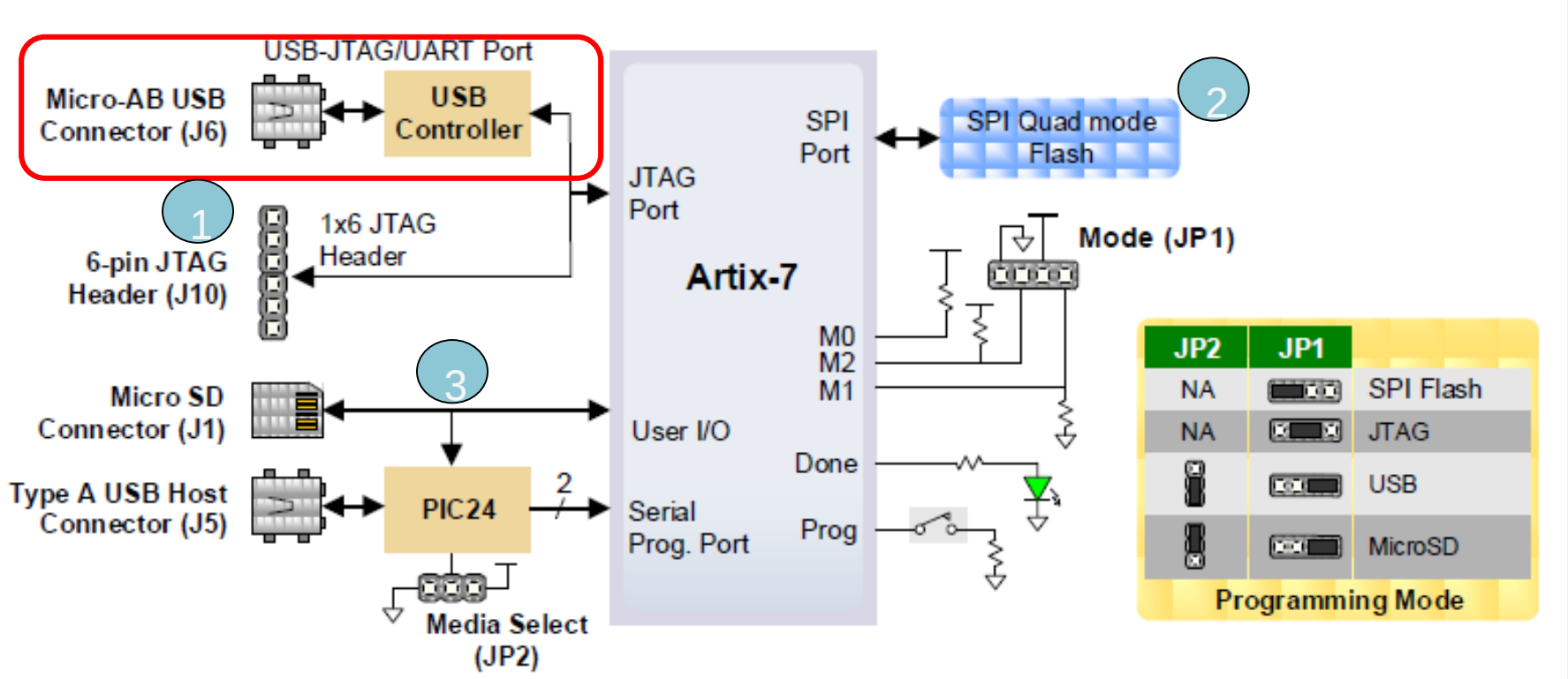
- Slave – FPGA configured by external source (i.e., a μP)
  - Serial or Parallel options
  - Used for dynamic reconfiguration
  - Can also read configuration memory contents
- Boundary Scan Interface
  - 4-wire IEEE standard serial interface for testing
  - Write and read access to configuration memory
    - Not available in all FPGAs
    - Used for dynamic partial reconfiguration
  - Interfaces to FPGA core
    - Not available in all FPGAs
    - Connections between Boundary Scan Interface and internal routing network and PLBs (Xilinx provides 2-4 of these ports)
- Other configuration interfaces in some FPGAs

Slave configuration modes



Nexys4 DDR configuration options

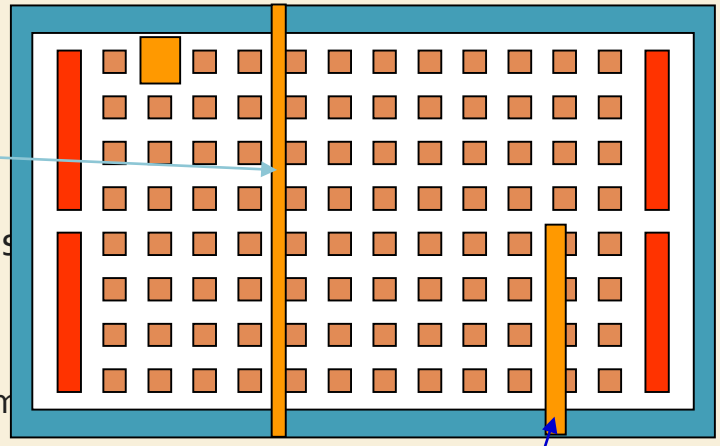
Artix-7 100T bitstream is typically 30,606,304 bits



1. USB-JTAG : PC connection via USB or JTAG
2. Master SPI: Program from "quad mode" flash memory (x1, x2, x4 width)
3. USB/SD: Program from micro SD card or USB memory stick

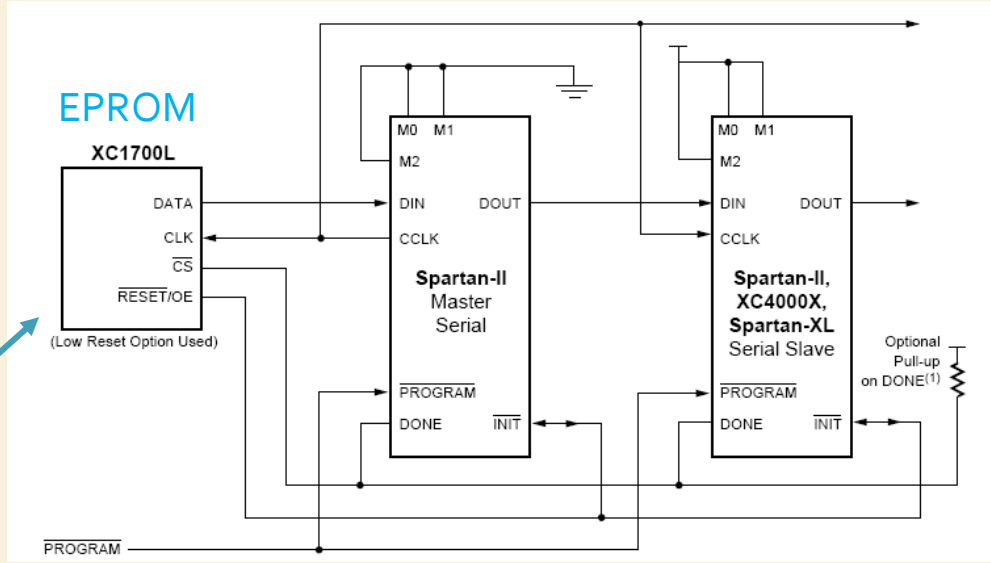
FPGA Configuration Memory

- PLB addressable
  - Good for partial reconfiguration
  - X-Y coordinates of PLB location to be written
    - Requires tag to identify which resources will be configured
- Frame addressable
  - Vertical or horizontal frame
  - Access to all PLBs in frame
    - Only portion of logic and routing resources acces
    - Many frames to configure PLBs
      - Major address for column, minor address for fram



Hybrid, i.e.:
Virtex-4
Virtex-5
Virtex-6

Daisy Chain Configuration



Configuration Bits

Xilinx Configuration Interface Pins

Name	Direction	Driver Type	Description
Dedicated Pins			
CCLK	Input/Output	Active	Configuration clock. Output in Master mode.
$\overline{\text{PROGRAM}}$	Input		Asynchronous reset to configuration logic.
DONE	Input/Output	Active/ Open-Drain	Configuration status and start-up control.
M2, M1, M0	Input		Configuration mode selection.
TMS	Input		Boundary-scan tap controller.
TCK	Input		Boundary-scan clock.
TDI	Input		Boundary-scan data input.
TDO	Output	Active	Boundary-scan data output.
Dual Function Pins			
DIN (D0)	Input/Output	Active Bidirectional	Serial configuration data input.
D[0:7]	Input/Output	Active Bidirectional	Slave Parallel configuration data input, readback data output.
$\overline{\text{CS}}$	Input		Chip Select (Slave Parallel only).
$\overline{\text{WRITE}}$	Input		Active Low write select, read select (Slave Parallel only).
BUSY/ DOUT	Output	Open-Drain/ Active	Busy/$\overline{\text{Ready}}$ status for Slave Parallel (open-drain). Serial configuration data output for serial daisy-chains (active).
$\overline{\text{INIT}}$	Input/Output	Open-Drain	Delay configuration, indicate configuration clearing or error.

Configuration Techniques

- Full configuration & readback
  - Simple configuration interface
    - Internal automatic calculation of frame address
  - Long download time for large FPGAs
- Partial reconfiguration & readback
  - Only change portions of configuration memory with respect to reference design
    - Reduces download time for reconfiguration
  - Requires more complicated interface
    - Command Register (CMR)
    - Frame Length Register (FLR)
    - Frame Address Register (FAR)
    - Frame Data Register
      - Input (FDRI) – for download
      - Output (FDRO) – for readback (*note separate access*)

Full Configuration Example

- Dummy Word 0xFFFFFFFF
- Synchronize Word 0xAA995566
- CMD Write 0x30008001
  - Reset CRC 0x00000007
- FLR Write 0x30016001
  - FLR = 0x00000024
  - Frame length = 37 words
    - 1,184 bits ÷ 32 bits/word
- COR Write 0x30012001
  - COR Write 0x00003FE5
- IDCODE Write 0x3001C001
  - Device ID = 0x0140D093 (3S50)
- MASK Write 0x3000C001
  - MASK = 0x00000000
- CMD Write 0x30008001
  - Switch CCLK 0x00000009
- FAR Write 0x30002001
  - FAR = 0x00000000 (full config)
- CMD Write 0x30008001
  - Write CFG 0x00000001
- FDRI Write 0x30004000
  - # words to write 0x50003555

Xilinx ASCII Bitstream
Created by Bitstream I.32
Design name: s3mod7.ncd
Architecture: spartan3
Part: 3s50tq144
Date: Tue Sep 04 15:50:09 2007
Bits: 439264

```
11111111111111111111111111111111
10101010100110010101010101100110
00110000000000001000000000000001
00000000000000000000000000000111
00110000000000010110000000000001
00000000000000000000000000100100
00110000000000010010000000000001
01000000000000000011111111100101
00110000000000011100000000000001
00000001010000001101000010010011
00110000000000011000000000000001
00000000000000000000000000000000
00110000000000010000000000000001
00000000000000000000000000001001
00110000000000000100000000000001
00000000000000000000000000000000
00110000000000010000000000000001
00000000000000000000000000000001
00110000000000001000000000000000
01010000000000000110101010101010
```

start of actual configuration data