# Digital System on Chip (SoC) Computer-Aided Design Flow

ELEC 4200 – Digital Systems Design

Victor P. Nelson

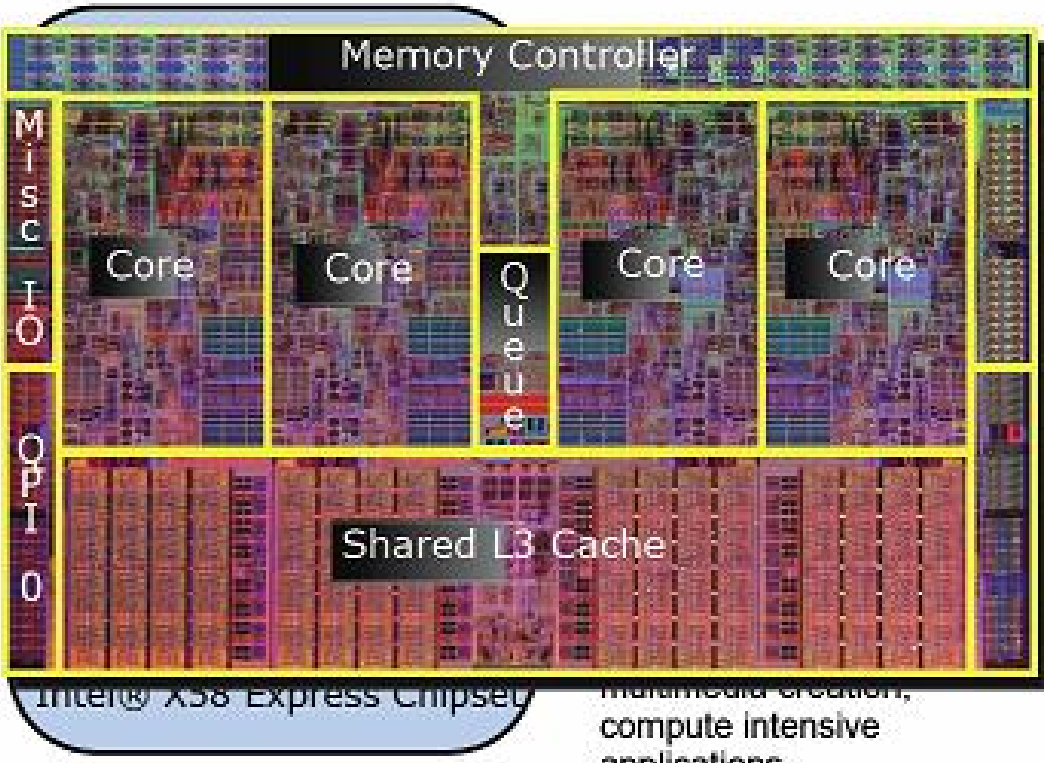
# Progress of State of the Art

| Year | Integration Level | # devices | Function |
|---|---|---|---|
| 1938-46 | Electromagnetic relays | 1 | |
| 1943-54 | Vacuum tubes | 1 | |
| 1947-50 | Transistor invented | 1 | |
| 1950-61 | Discrete components | 1 | |
| 1961-66 | SSI | 10's | Flip-flop |
| 1966-71 | MSI | 100's | Counter |
| 1971-80 | LSI | 1,000's | uP |
| 1980-85 | VLSI | 100,000's | uC |
| 1985-90 | ULSI* | 1M | uC* |
| 1990 | GSI** | 10M | SoC |
| 2011 | Intel Ten-Core Xeon | 2.6G | CPU |
| 2017 | Nvidia GV100 Volta | **21.1G** | GPU |

# Intel® Core™ i7 Processor

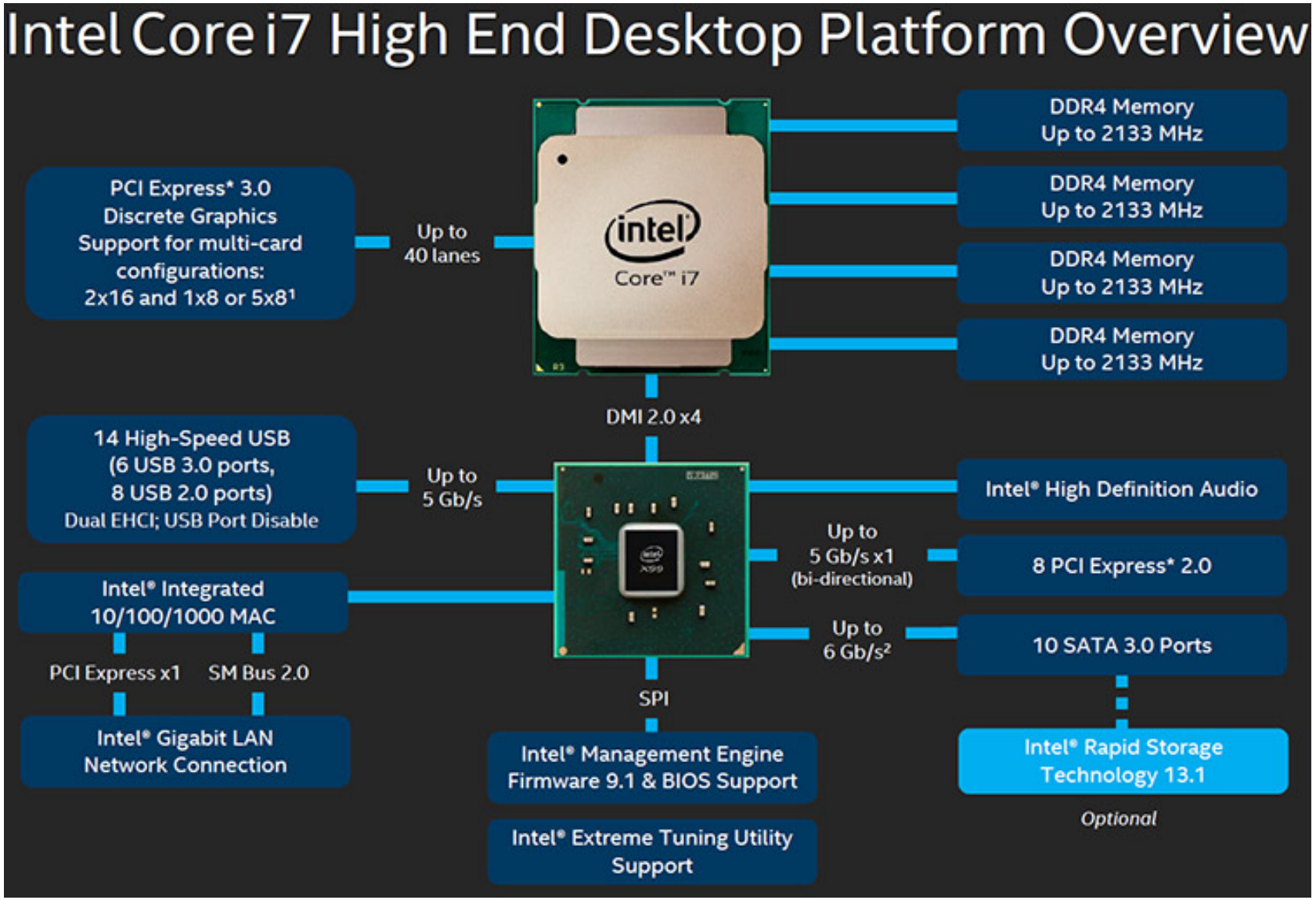
**Performance/Features:**

- 8 processing threads via Intel® Hyper-Threading Technology (HT)
- 4 cores
- Turbo Mode operation
- Intel® QuickPath Interconnect (Intel® QPI) to Intel® X58 Express Chipset
- Integrated Memory Controller (IMC) – 3ch DDR3
- 7 more SSE4 instructions
- Overspeed Protection Removed



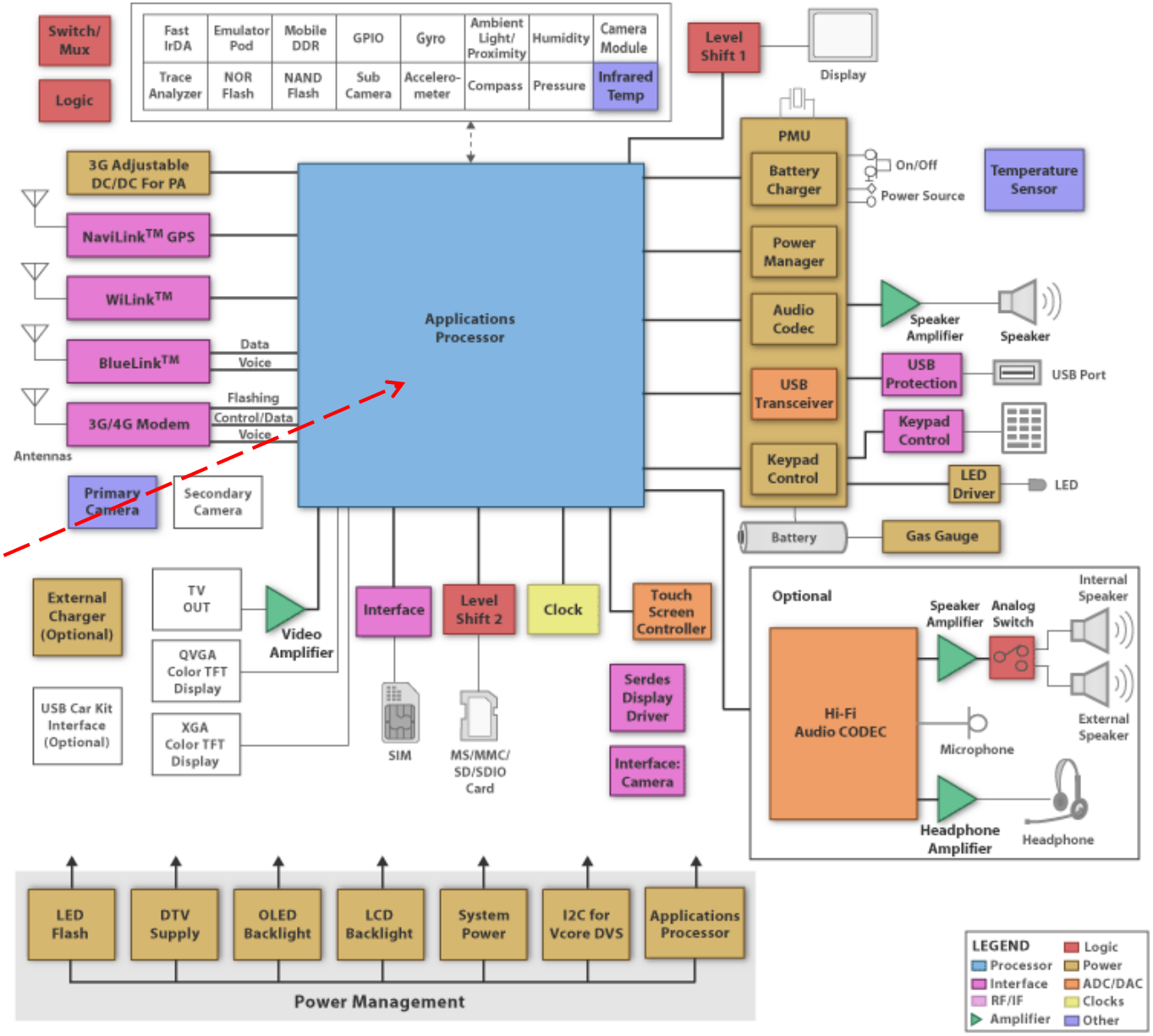

compute intensive applications

**Intel's Next Gen Computing Genius!**


Intel Core i7 High End Desktop Platform Overview
PCI Express* 3.0
Discrete Graphics
Support for multi-card
configurations:
2x16 and 1x8 or 5x8[1]
Up to
40 lanes
intel
Core™ i7
DDR4 Memory
Up to 2133 MHz
DDR4 Memory
Up to 2133 MHz
DDR4 Memory
Up to 2133 MHz
DDR4 Memory
Up to 2133 MHz
DMI 2.0 x4
14 High-Speed USB
(6 USB 3.0 ports,
8 USB 2.0 ports)
Dual EHCI; USB Port Disable
Up to
5 Gb/s
Intel® High Definition Audio
Up to
5 Gb/s x1
(bi-directional)
8 PCI Express* 2.0
Intel® Integrated
10/100/1000 MAC
Up to
6 Gb/s[2]
10 SATA 3.0 Ports
PCI Express x1
SM Bus 2.0
SPI
Intel® Gigabit LAN
Network Connection
Intel® Management Engine
Firmware 9.1 & BIOS Support
Intel® Rapid Storage
Technology 13.1
Optional
Intel® Extreme Tuning Utility
Support

# T.I . smartphone reference design

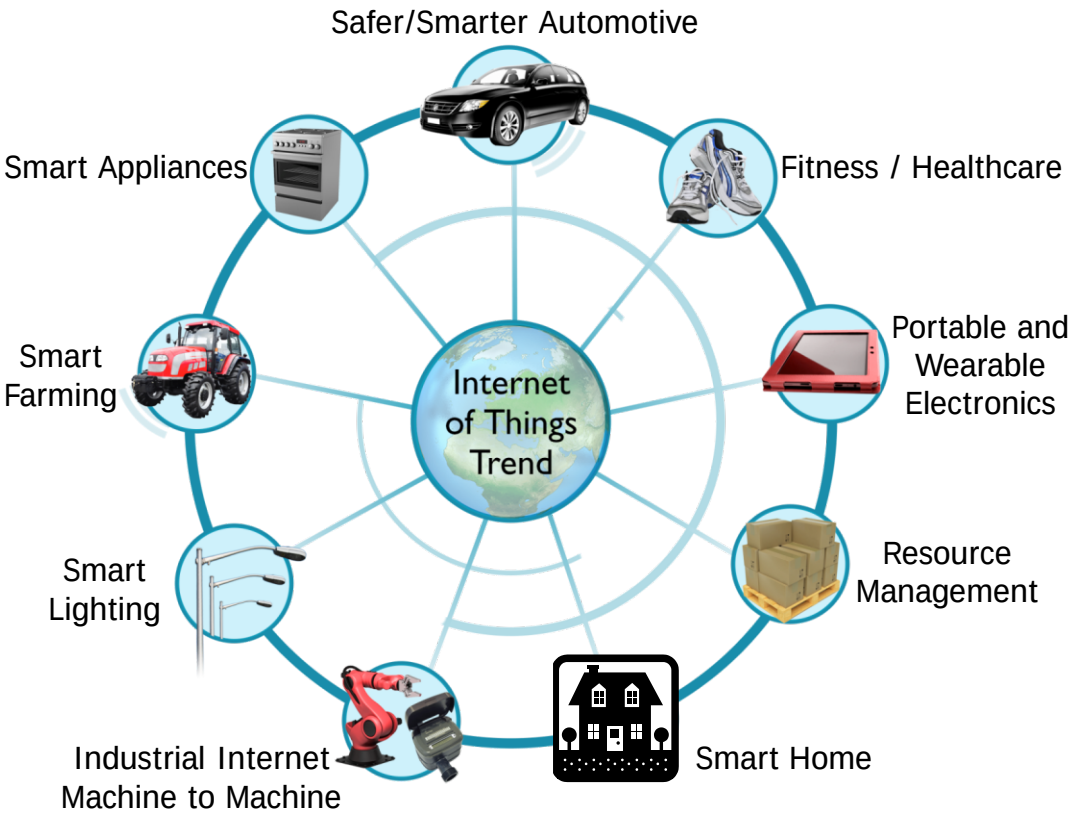
Main SoC



# Apple "A8" SoC (System on Chip)

- Used in *iPhone6 & iPhone6 Plus*
- Manufactured by TSMC
  - *20nm, 89mm$^2$, 2B transistors*
- *Elements (unofficial):*
  - *2 x ARM Cyclone ARMv8 64-bit cores running at 1.4GHz*
  - *IMG PowerVR 4-core GX6450 GPU*
  - *L1/L2/L3 SRAM caches*
- *Other devices*
  - *1 GB LPDDR3 SDRAM*
  - *16 to 128GB flash*
  - *Qualcomm MDM9625M LTE modem*
  - *M8 motion coprocessor (ARM Cortex M3 uC)*
  - *iSight camera*
  - *Near field communications chip (for Apple Pay)*
  - *User interface and sensors, accelerometers, gyro*
  - *Wi-Fi and Bluetooth*

# Internet of Things (IoT)




## Socio-Economic Benefits

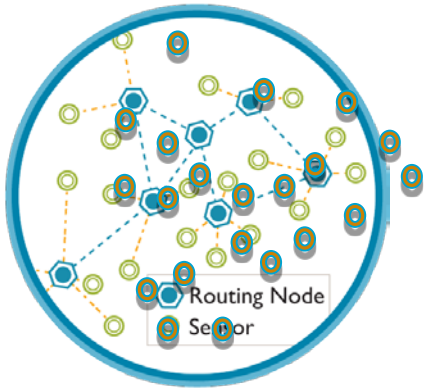
- Automation (higher productivity)
- Smart monitoring, control and maintenance (higher efficiency, lower cost, higher quality, better optimisation/outcomes)
- Better safety (early warning)
- Higher responsiveness (dynamic response to varying demands)
- Huge and varied applications in industry, agriculture, health, transport, infrastructure, smart living, consumer etc.

# IoT: Connecting the Physical and Digital Worlds

Sensing and Controlling

- Integrated sensors, memory and processing
- Low power systems
- Little Data

Things (“Edge” Devices)



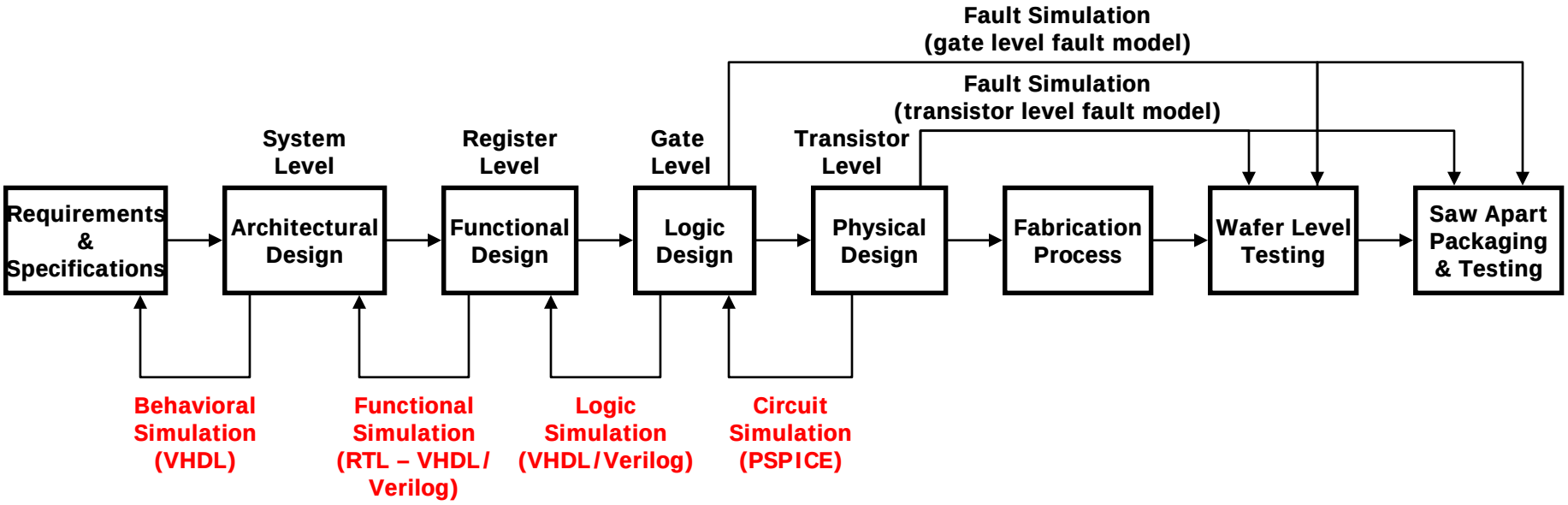

Wireless Network

- High throughput networks
- Low power wireless networks

Cloud

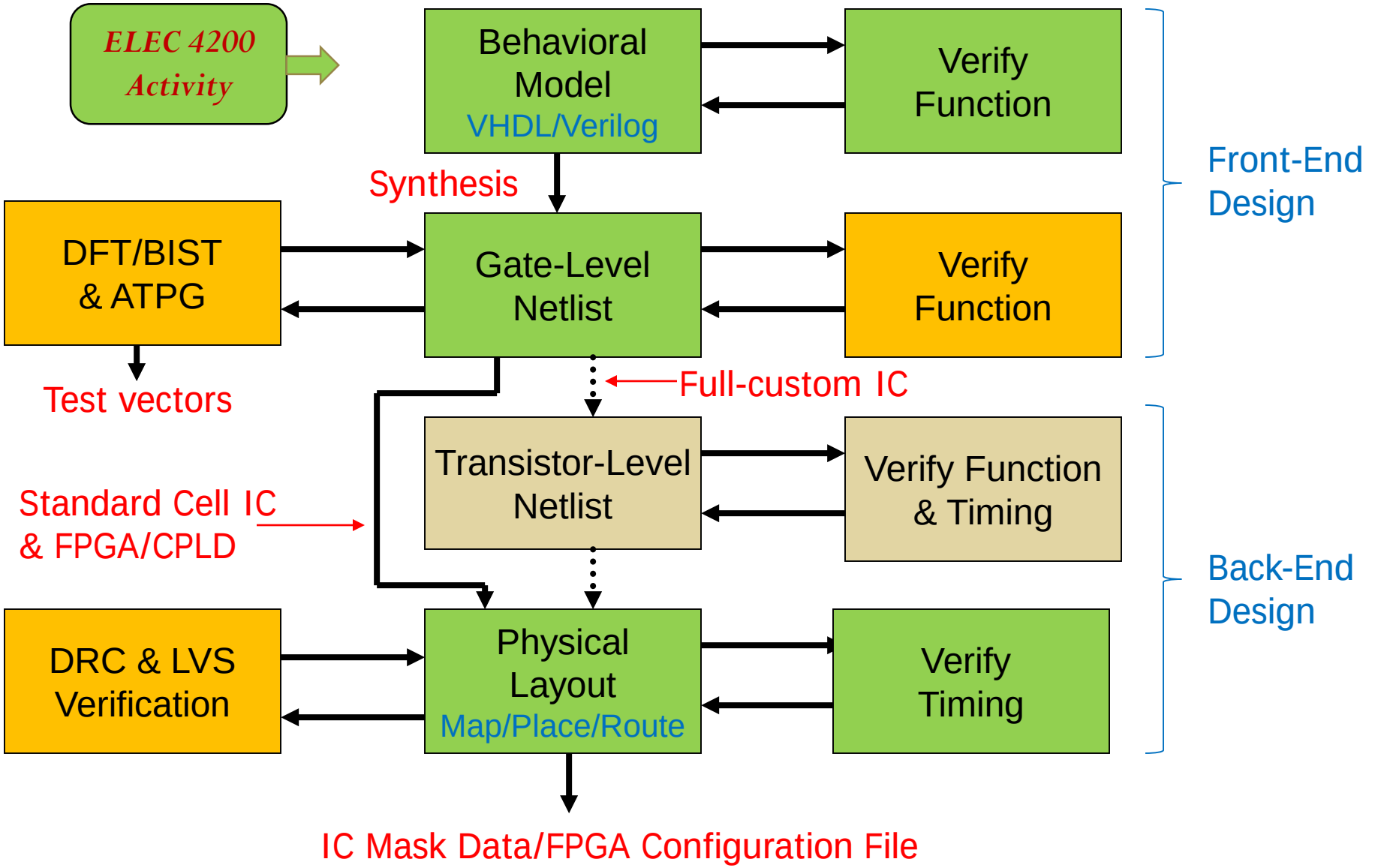
- High performance efficient servers
- High capacity storage
- Software as a service
- Big Data

# Digital integrated circuit design process




- **Note all the simulation** (design verification) - helps to ensure the design works and assists in debugging design errors
- To simulate a circuit, we must describe it in a manner that can be interpreted and understood by the simulator (HDL/netlist)

# Digital ASIC Design Flow

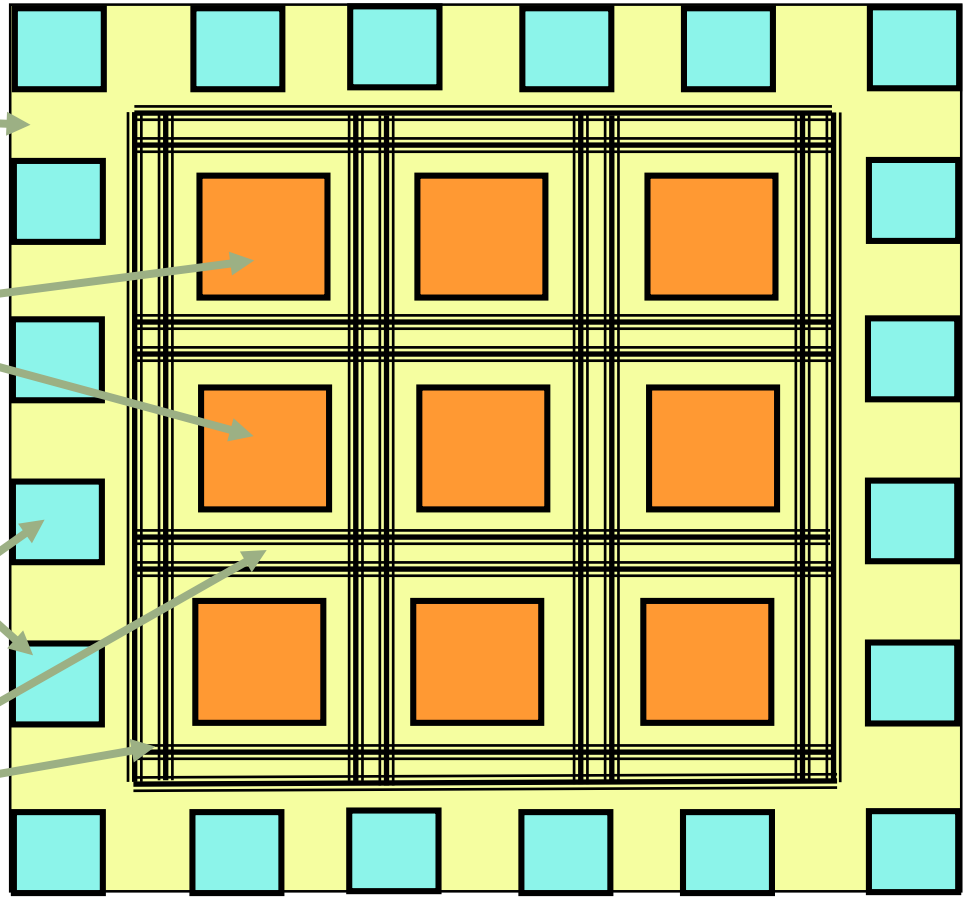


# Xilinx/Altera FPGA/CPLD Design Tools

- Create HDL model of design behavior/structure
  - Xilinx "***Vivado***" - *Integrated Software Environment*
  - Context-sensitive text editor
- Simulate designs in *Active-HDL or Modelsim*
  - Behavioral models (VHDL, Verilog)
  - Synthesized netlists (VHDL, Verilog)
    - Requires "primitives" library for the target technology
- Synthesize primitive-level netlist from a behavioral model
  - *Xilinx* ***Vivado*** has its own synthesis tool (*Xilinx ISE* for older FPGAs)
  - *Leonardo (Levels 1,2,3)* has libraries for most FPGAs (ASIC-only version currently installed)
- Vendor tools for back-end design
  - Map, place, route, configure device, timing analysis, generate timing models
  - Xilinx ***Vivado*** - formerly *Integrated Software Environment* (ISE)
  - Altera *Quartus II & Max+Plus2*
- Higher level tools for system design & management
  - *Xilinx Platform Studio :* SoC design, IP management, HW/SW codesign
  - Mentor Graphics *FPGA Advantage*

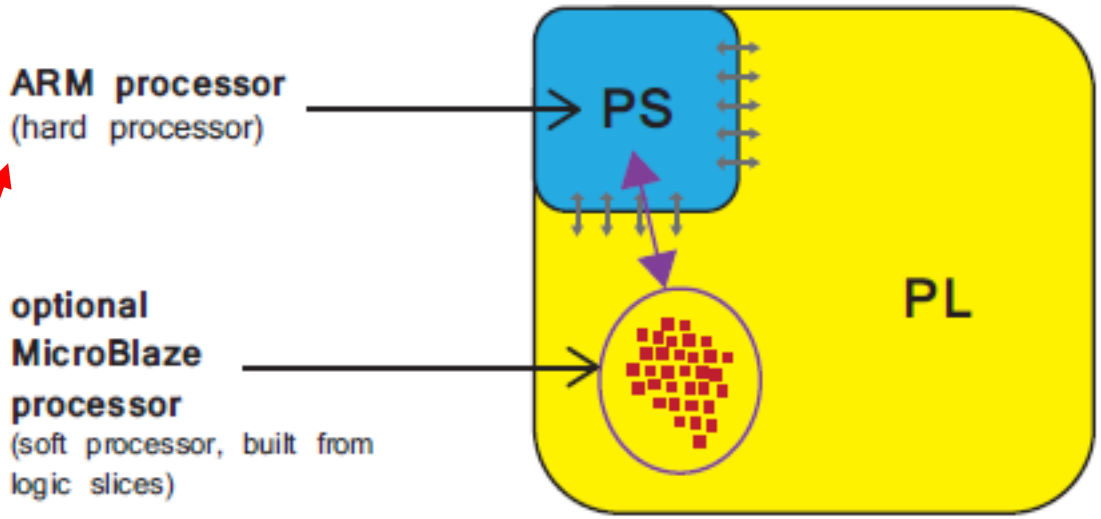
# Field Programmable Gate Arrays

- Configuration Memory
- Programmable Logic Blocks (PLBs)
- Programmable Input/Output Cells
- Programmable Interconnect



Typical Complexity = 5M – 1B transistors

# Xilinx Zynq SoC devices



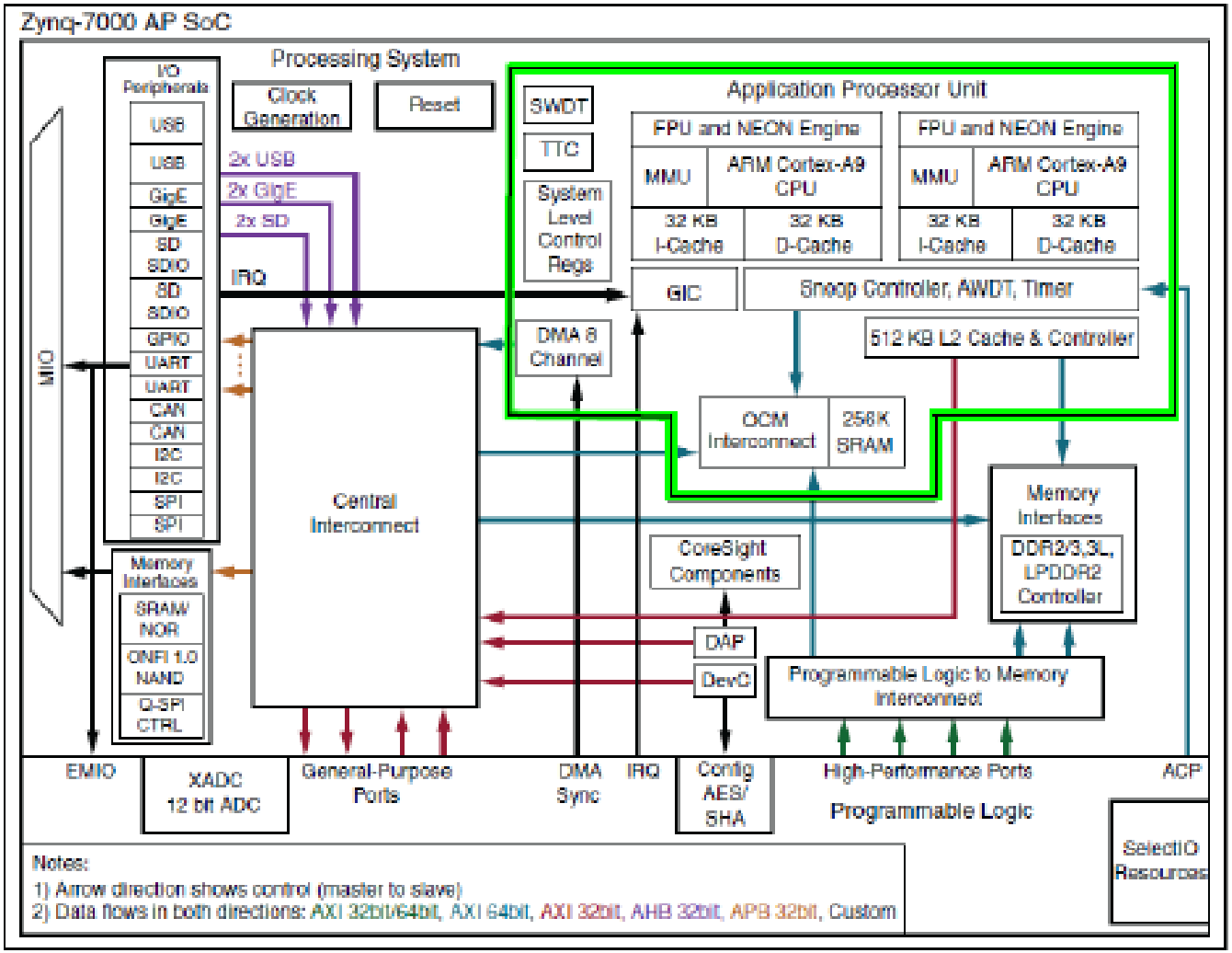

PL = Programmable Logic

Zynq-7000 SoC: Dual-core ARM Cortex-A9 MPCore (up to 1GHz)

Zynq UltraScale+ MPSoC:

- Quad-core ARM Cortex-A53 MP (up to 1.5 GHz)
- Dual-core ARM Cortex-R5 MPCore (up to 600MHz)
- GPY ARM Mali-400 MP2 (up to 667MHz)

# Zynq-7000 SoC Processor System



# Xilinx FPGA families (2015)

| | Spartan-6 | Artix-7 | Kintex-7 | Virtex-7 | Kintex UltraScale | Virtex UltraScale |
|---|---|---|---|---|---|---|
| Logic Cells | 147,443 | 215,360 | 477, 760 | 1,954,560 | 1,160,880 | 4,432,680 |
| BlockRAM | 4.8Mb | 13Mb | 34Mb | 68Mb | 76Mb | 132.9Mb |
| DSP Slices | 180 | 740 | 1,920 | 3,600 | 5,520 | 2,880 |
| DSP Performance (symmetric FIR) | 140GMACs | 930GMACs | 2,845GMACs | 5,335GMACs | 8,180 GMACs | 4,268 GMACs |
| Transceiver Count | 8 | 16 | 32 | 96 | 64 | 120 |
| Transceiver Speed | 3.2 Gb/s | 6.6 Gb/s | 12.5 Gb/s | 28.05 Gb/s | 16.3 Gb/s | 32.75 Gb/s |
| Total Transceiver Bandwidth (full duplex) | 50 Gb/s | 211 Gb/s | 800 Gb/s | 2,784 Gb/s | 2,086 Gb/s | 5,886 Gb/s |
| Memory Interface (DDR3) | 800 | 1,066 | 1,866 | 1,866 | 2,400 | 2,400 |
| PCI Express® Interface | x1 Gen1 | x4 Gen2 | x8 Gen2 | x8 Gen3 | x8 Gen3 | x8 Gen3 |
| Analog Mixed Signal (AMS)/XADC | - | XADC | XADC | XADC | System Monitor | System Monitor |
| Configuration AES | Yes | Yes | Yes | Yes | Yes | Yes |
| I/O Pins | 576 | 500 | 500 | 1,200 | 832 | 1,456 |
| I/O Voltage | 1.2V – 3.3V | 1.2V – 3.3V | 1.2V – 3.3V | 1.2V – 3.3V | 1.0 – 3.3V | 1.0 – 3.3V |

**Digikey.com (4/03/18):**

Spartan-3A XC3S50A: $8.05

Spartan-6 XC6SLX4: $11.48

Artix-7 XC7A100T: $136.50

Kinetix-7 XC7K70T: $139.65

Virtex7 XC7V1140T-G2FLG1925E: $32,815.17

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Digikey.com (1/14/15):
Spartan-3A XC3S50A: $6.44
Spartan-6 XC6SLX4: $11.48
Artix-7 XC7A100T: $125.58; XC7A200T: $186.25
Kinetix-7 XC7K70T: $133.90; XC7K480T: $2,908.75
Virtex7 XC7V2000T-G2FLG1925E: $39,452.40