

Post-Implementation Timing Simulation



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Objectives

- This tutorial will show you how to run a Post-Implementation timing simulation with Xilinx Vivado and Aldec Active-HDL

Simulation Settings

- In Vivado, after you have implemented your design, click on “Simulation Settings”.

The screenshot displays the Vivado 2016.2 interface for project LAB04. The left-hand 'Project Manager' pane shows the 'Simulation' section expanded, with 'Simulation Settings' highlighted by a red box. The main workspace is divided into several panels:

- Project Manager - LAB04:** Shows a tree view of sources including Design Sources (MooreFSM - Behavioral), Constraints (constrs_1), and Simulation Sources (LAB04_Constraints.xdc).
- Properties:** A table showing properties for MooreFSM.vhd:

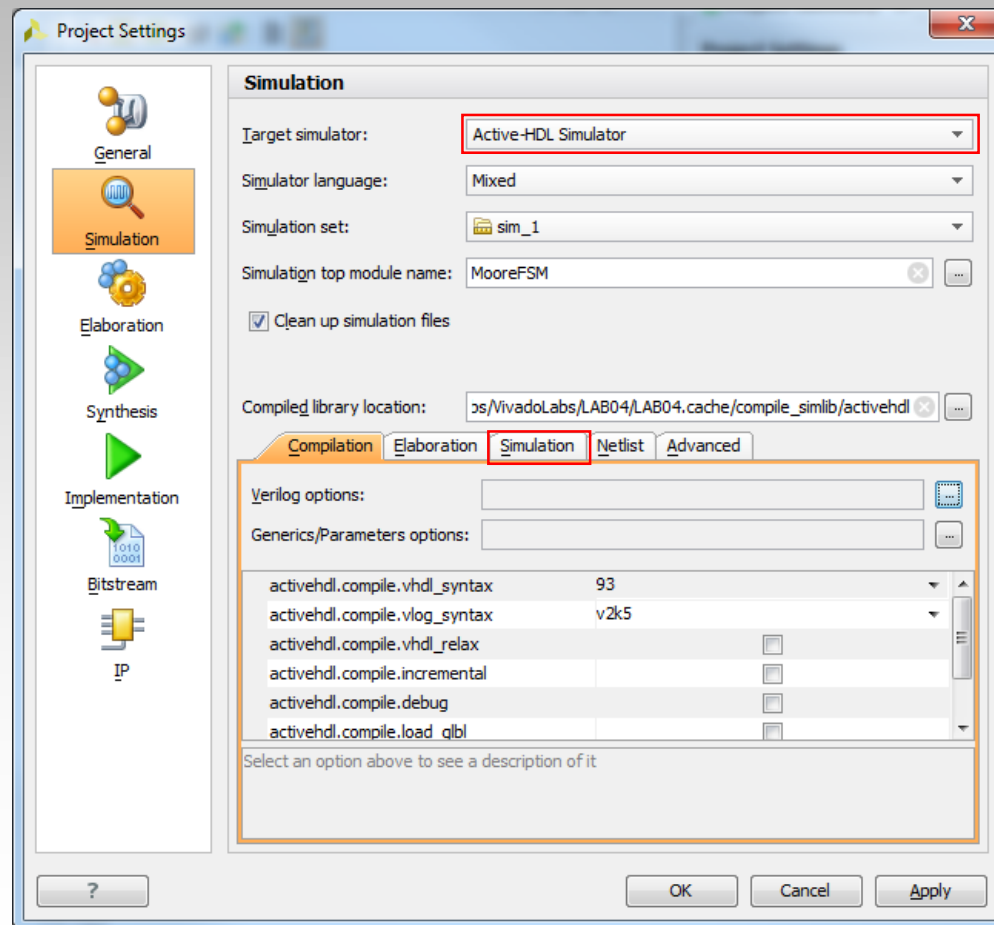
CLASS	file
CORE_CONTAINER	
FILE_TYPE	VHDL
IS_AVAILABLE	<input checked="" type="checkbox"/>
IS_ENABLED	<input checked="" type="checkbox"/>
IS_GENERATED	

- Project Summary:** Displays project settings such as Project name (LAB04), Project location, Product family (Artix-7), Project part (xc7a100tcsq324-1), Top module name (MooreFSM), Target language (VHDL), and Simulator language (Mixed).
- Synthesis:** Shows a status of 'Complete' with 'No errors or warnings' and a strategy of 'Vivado Synthesis Defaults'.
- Design Runs:** A table listing the results of synthesis and implementation runs:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF
synth_1	constrs_1	synth_design Complete!								6
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	6

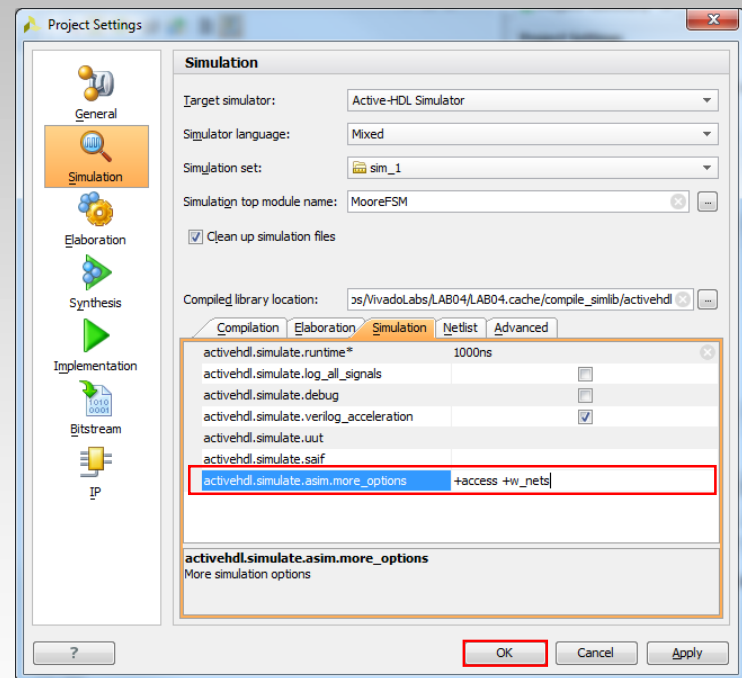
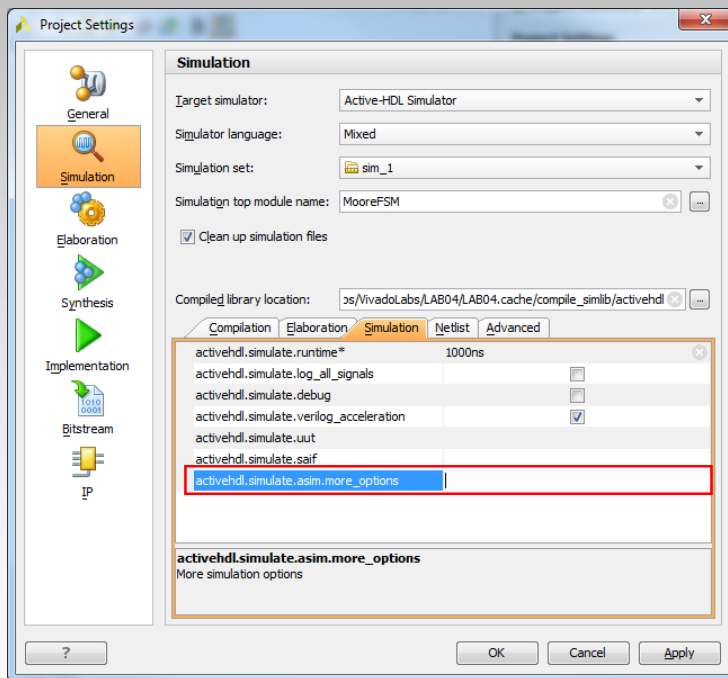
Selecting the Simulator

- First, make sure that the Target Simulator is set to (Aldec) Active-HDL Simulator.
- Next, click on the “Simulation Tab”



Simulator Options

- Click in the box next to ***activehdl.simulate.asim.more_options*** and type “+access +w_nets” without the quotation marks.
- Click “OK” or “Apply” and close the window.



Running the Simulation

- Now, click on “Run Simulation” and select “Run Post-Implementation Timing Simulation”

The screenshot displays the Vivado 2016.2 IDE interface for a project named LAB04. The 'Run Simulation' option in the left-hand 'Simulation' menu is expanded, showing a list of simulation types. The 'Run Post-Implementation Timing Simulation' option is highlighted with a red box. The 'Project Summary' window on the right provides details about the project, including its name, location, product family (Artix-7), and part number (xc7a100tcsq324-1). The 'Synthesis' status is 'Complete', and the 'Implementation' status is also 'Complete'. The 'Design Runs' table at the bottom shows the progress of the synthesis and implementation steps.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BR
synth_1	constrs_1	synth_design Complete!							6	5	
impl_1	constrs_1	write_bitstream Complete!	8.582	0.000	0.224	0.000	0.000	0	6	5	

Running the Simulation

- Remove the internal signals from the waveform (unless you need them for some reason) and set up the stimulators as you normally would.
- Observe the differences between the behavioral and timing simulations.

The screenshot displays the Active-HDL Student Edition interface. The top menu bar includes File, Edit, Search, View, Workspace, Design, Simulation, Waveform, Tools, Window, and Help. The main window is divided into several panes:

- Design Browser:** Shows a hierarchy with 'MooreFSM' and 'glbl'.
- Signal name Value:** A table listing signals and their current values. A cursor is positioned at 160 ns.
- Waveform:** A timing diagram showing signals over time. A cursor is at 160 ns.
- Console:** Shows simulation logs.

Signal name	Value
CLK	z
CLK_IBUF	x
CLK_IBUF_BUFG	x
Cout	0
Cout_OBUF	0
FSM_sequential_C[...]	0
FSM_sequential_C[...]	0
Oout	7
Oout_OBUF	7
PB	z
PB_IBUF	x
RST	z
RST_IBUF	x
X	0
Y	0
Z	0

```
o # Simulation has been initialized
o # 16 signal(s) traced.
o # Waveform file 'untitled.awc' connected to
  'C:/Users/jar0012/Dropbox/GTA_Stuff/ELEC_4200/Lab_Material/Labs/VivadoLabs/LAB04/LAB04.sim/sim_1/impl/timing/LAB04/src/wave.as
db'.
o # KERNEL: stopped at time: 1 us
```