ELEC 4200 Lab#7
Hierarchical Modeling & Synthesis

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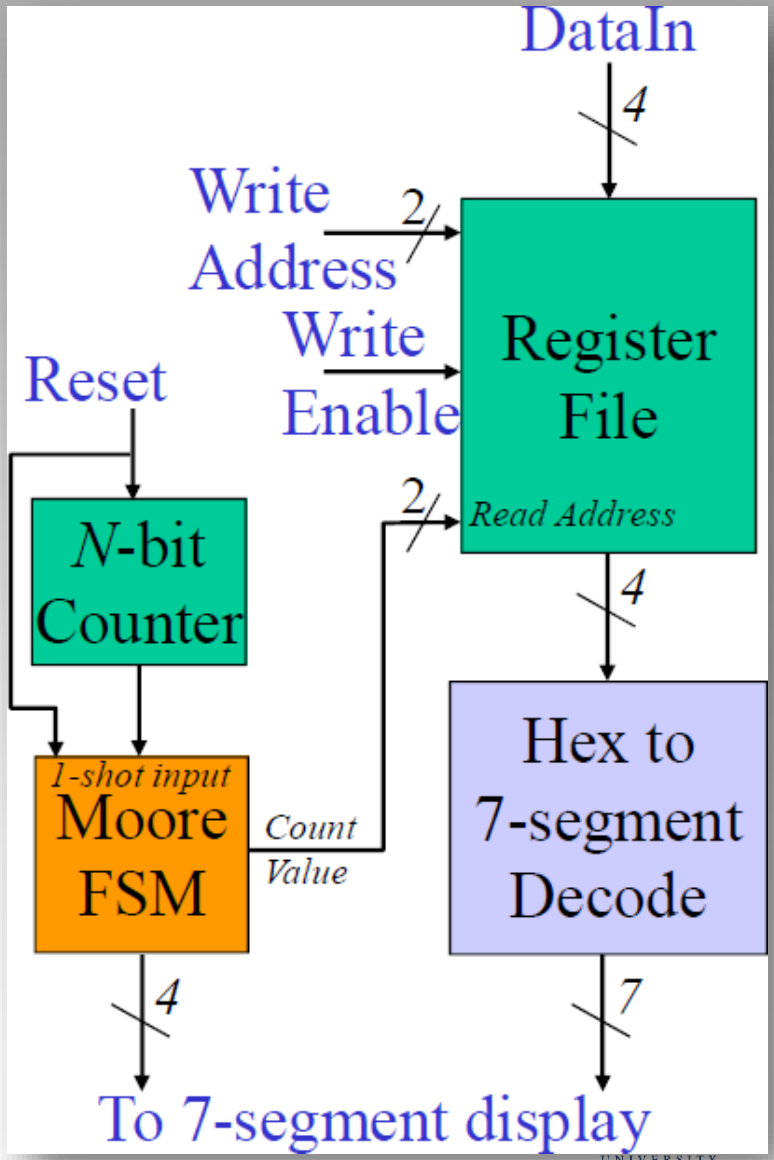
Specifications(1)

- Write a top-level VHDL model to combine your previous models
  - Hex to 7-segment decoder (Lab 3)
  - Moore FSM (Lab 4)
  - N-bit counter (Lab 5)
  - Register File (Lab 6)
- Note: The block diagram is not complete and only shows signals that connect in-between the different models.



Specifications(2)

- The overall circuit will be a time-multiplexed display that will display data individually to the four 7-segment displays
- Design specs
  - Hex to 7-segment decoder will convert value from the register file and supplied the A-G values to the 7-segment display
  - The Register file will take write address, data, and write enable inputs from switches (address, data) and a push button (write enable)
  - The N-bit counter MSB will supply the enable input to the FSM to advance the FSM every 2^N clock cycles
    - Your FSM should already contain the one shot
    - Use the parameterized register/counter with inputs tied such that the model is always counting.
  - The Moore FSM will supply
    - Active LOW enables (AN0-3) to 7 segment display to cycle through the four displays
    - Read address (count value) to the register file.
  - Clock input for FSM and counter will come from the 100Mhz oscillator

Pre-lab Assignment

- Write a top level VHDL model to combine your previous VHDL models as per the specifications
- Determine the FPGA pin numbers for register file inputs
  - Address and Data inputs from DIP switches
  - Write Enable from Push Button

Lab Exercise(1)

- Simulate your VHDL model and verify your design using Aldec Active-HDL.
  - Set the Register File generic values to M=2 and N=4 for design verification.
- Synthesize and implement your design for the Artix-7 FPGA on the Nexys4 board.

Lab Exercise(2)

- You will have to experiment with the “N” value for the N-bit counter to find a speed at which the display multiplexes at a reasonable speed.
  - The display should be fast enough such that all four displays appear on at the same time, but should be slow enough to prevent blurring
  - Use the range 8<N<25 for a starting point.
- From the implementation report record the number of Slices, LUTs, and FF/latches for each value of the N-bit counter you try.
- Download your design to the FPGA and demonstrate the working circuit to the GTA

Report Guidelines

- Be sure to include all sections required by the lab manual guidelines. In addition be sure your report includes the following:
  - Verified VHDL model (Top-level and any changes needed to other models)
  - Annotated screenshots of your Aldec Active-HDL simulation results.
  - Synthesis results (LUTs, FFs, slices, etc)
  - Value of N used for the counter
  - Answers to the following questions…

1. Do you think it would have been faster to create the circuit as an integrated solution instead of component by component?

2. Which would be easier when it comes to debugging the circuit?