AUBURN
UNIVERSITY

SAMUEL GINN
COLLEGE OF ENGINEERING

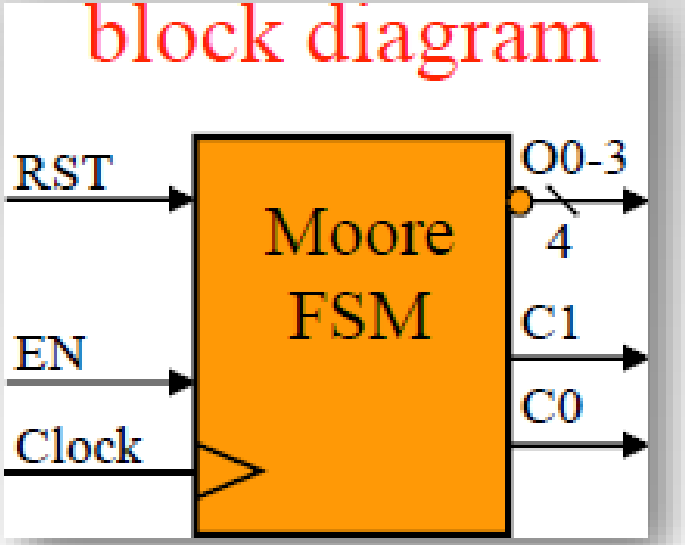
ELEC 4200 Lab#4 VHDL Modeling and Synthesis of Sequential Logic Design

- References you may need:
  - Viewing and Editing Designs in Vivado.pdf
  - Post-Implementation Timing Simulation.pdf
  - **Lab #2**

AUBURN
UNIVERSITY
SAMUEL GINN
COLLEGE OF ENGINEERING

Specifications

- Write a VHDL behavioral model for the FSM from Lab 2
  - Use the same specification as in Lab 2
  - Make sure it includes the digital one-shot
  - Use any valid sequential and concurrent statements
  - Do not use the Boolean equations from lab 2
- In addition to the normal behavioral simulation, you will perform a post-implementation timing simulation.



Pre-lab Assignment

- Write a VHDL behavioral model for your design.
  - Reminder: Include the digital one-shot
- If needed, review the “Viewing and Editing Designs in Vivado” tutorial on the class website

Lab Exercise (1)

- Simulate your VHDL model with Aldec Active-HDL
- Synthesize, implement, download, and verify your design on the Nexys4 board
  - Record the number of LUTs, FF/latches, slices, and maximum clock frequency from the implementation report
  - Open your implemented design in Vivado and try to determine how your design was synthesized (what state encoding was used, did the synthesizer use any special functions such as shift register or counters, etc.) Sometimes Vivado can be be a little cryptic when showing how the circuit was synthesized so ask the GTA if you are having a hard time.
- Demonstrate your working circuit to the GTA

Lab Exercise (2)

- Simulate the post-implementation timing model
  (Refer to: **Post-Implementation Timing Simulation.pdf**)
  - In the Project Manager, click on ***Run Simulation*** and select ***Run Post-Implementation Timing Simulation*** from the list of options.
- Simulate the model using Aldec Active-HDL
- Compare timing delays in the simulation to the original behavioral VHDL simulation
- From the Vivado Project Summary window, open the "Implemented Timing Report"
  - Click on the "worst negative slack" value to find information about the circuit paths with the longest delays
  - Determine if the circuit can be operated at a higher clock rate.
  - Open a Schematic Window, and click on the worst-case path to see that path in the implemented circuit.

Report Guidelines

- Ensure that you include all sections required by the lab manual guidelines. In addition ensure that your report includes the following:
  - Verified VHDL model
  - Annotated screenshots of your Aldec Active-HDL simulation results
    - Functional simulation
    - Post-Implementation timing simulation
  - Post-implementation results (LUTs, FFs, slices, frequency)
  - Answers to the following questions…

1. What is the difference between the behavioral simulation and the post-implementation timing simulation?

2. From the simulation and the post-simulation timing report, what would be the shortest clock period (and/or highest clock frequency) at which the circuit could be reliably operated?