ELEC 4200 Lab#3
VHDL Modeling & Synthesis of 7-Segment Decoders

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- References you may need:
  - Viewing and Editing Designs in Vivado.pdf
  - **Lab #1**

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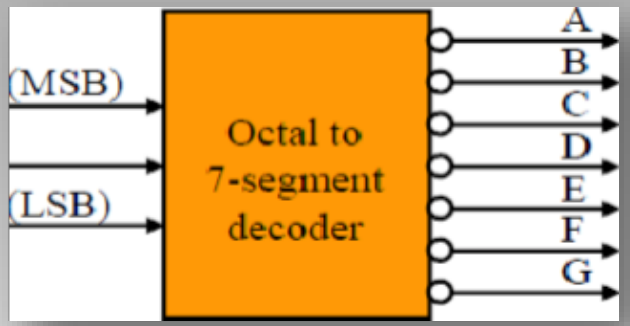
Specifications (1)

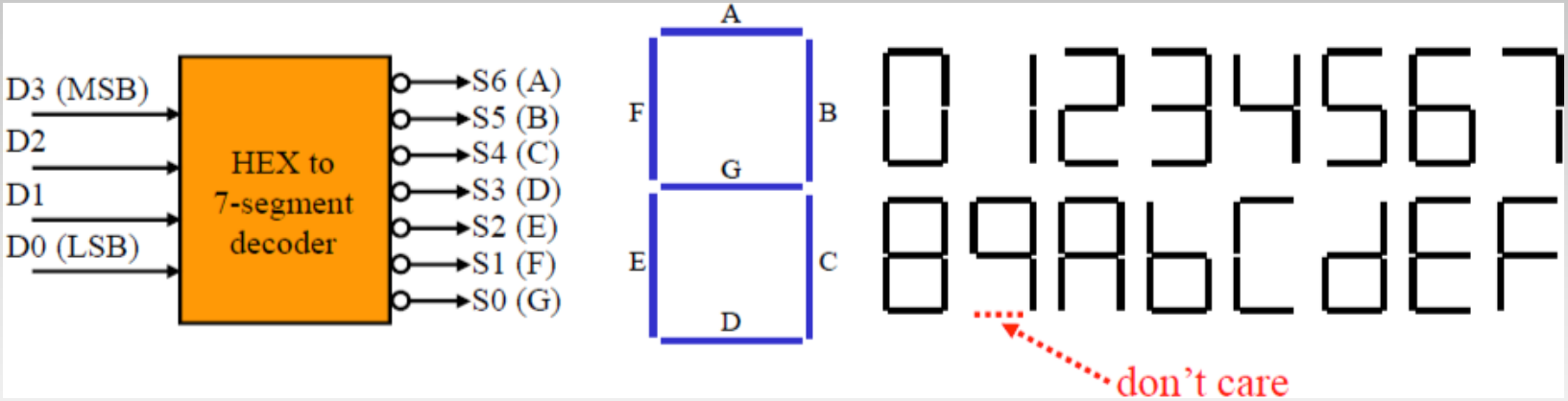
- Write a VHDL “behavioral” model for an octal to 7-segment decoder
  - Use specifications from Lab 1
  - Use a vector for the 3 inputs.
  - Use a vector for the 7-segment outputs



- Expand the octal to 7-segment decoder into a hex to 7-segment decoder
  - Hint: You should not have to re-do all the K-maps and logic equations that you derived in the pre-lab for Lab 1. Use what you know of VHDL modeling to make your life easier.
- You have to show the GTA both versions working on the hardware

Specifications (2)

- Use the following specifications for the Hex Decoder.



Pre-lab Assignment

- Write a complete VHDL “behavioral” model for the Octal to 7-segment decoder in Lab 1.
  - Do NOT use the Boolean logic equations from Lab1.
  - You may use any valid concurrent or sequential construct.
  - *Hint: When choosing, keep in mind that you will have to expand this to the HEX version.*
- Read “Viewing and Editing Designs in Vivado” on the class web page.

Lab Exercise

- For the Octal Decoder
  - Simulate your design in Aldec Active-HDL and debug your model as needed
  - Synthesize the model then double click “Report Utilization” under “Open Synthesized Design”
    - Record the number of slices, LUTs, and FF/Latches from the device utilization summary section
  - Run Implementation, then, referring to the “Viewing and Editing Designs in Vivado” tutorial, open your implemented design in Vivado and find the LUTs. Record the logic equation for each LUT
  - Download and verify the design onto the Artix-7 FPGA on the Nexys4 board.
    - Inputs → Switches
    - Outputs → 7-segment display
  - Show the working circuit to the GTA

Lab Exercise

- For the Hex Decoder
  - Repeat all of the same steps you did for the Octal Decoder EXCEPT finding the logic equations.

Report Guidelines

- Be sure to include all sections required by the lab manual guidelines. In addition be sure your report includes the following:
  - Both verified VHDL models
  - Annotated screenshot of your Aldec Active-HDL simulation results
    - Be sure to describe your testing method
  - Design work (if applicable)
  - Number of slices, LUTS, and FF/Latches for each design
  - Logic Equations from Vivado for the Octal decoder
  - Answers to the following questions…

1. **Explain** the number of LUTs used to implement the octal to 7-segment decoder and the hex to 7-segment decoder.

2. How to the synthesized logic equations for the octal to 7-segment decoder compare to the ones you manually derived in Lab 1?

Note: From here on out make sure you save all of your VHDL models as you will need them again later in the semester.