ELEC 4200 – DIGITAL SYSTEM DESIGN

Spring 2019 – Lecture: Tuesday/Thursday 8:00-8:50 a.m. in Broun 306
Lab in Broun 320: Section 001 Monday 4:00-6:50 p.m.
Section 002 Wednesday, 5:00-7:50 p.m.

Bulletin Data: **ELEC 4200. Digital System Design (3)** LEC. 2. LAB. 3. Pr. ELEC 2210 and ELEC 2220. Hierarchical, modular design of digital systems; synchronous and asynchronous sequential circuit analysis and design, programmable logic devices and field programmable gate arrays, and circuit simulation for design verification and analysis.

Textbook: *Digital Logic Circuit Analysis and Design, 2nd Ed. (**Draft**)*, V. P. Nelson, B. D. Carroll, H. T. Nagle, J. D. Irwin, Pearson Education, Inc. 2020, PDF file posted on Canvas course page.

References: On course web page: *http://www.eng.auburn.edu/~nelsovp/courses/elec4200/elec4200.html*

Coordinator: Victor P. Nelson, Professor of ECE, nelsovp@auburn.edu, Broun 326
GTAs: Michael Bolt, mtb0026@auburn.edu, Broun 407
Soham Roy, szr0075@auburn.edu, Broun 309

Course Goals:

1. To be able to analyze and design digital systems in a hierarchical, top-down manner.
2. To be able to model, simulate, verify, and synthesize digital systems using hardware description languages.
3. To be able to realize designs with programmable logic, including FPGAs

Prerequisites by topic:

1. Digital logic design and analysis
2. Digital electronics
3. Computer system organization and design

Course Outline:

Wk	Lecture Topic	Ch	Tentative Laboratory Projects
1	Overview of digital IC design and FPGAs Review of combinational logic circuits	**1**	**Lab 0:** Introduction to lab hardware and software
2	Review of sequential logic circuits, flip-flops and latches, timing analysis	**1**	**Lab 1:** Design capture, simulation and synthesis of combinational logic
3	VHDL syntax, entities, architectures	**2**	**Lab 2:** Design capture, simulation and synthesis of sequential logic
4	VHDL concurrent and sequential constructs	**2**	**Lab 3**: VHDL modeling, simulation and synthesis of combinational logic
5	VHDL modeling guidelines and parameterization, **Test #1**	**2**	**Lab 4:** VHDL modeling, simulation and synthesis of sequential logic
6	VHDL hierarchical design and test benches	**2**	**Lab 5:** VHDL parameterized modeling, simulation and synthesis of a universal register/counter
7	VHDL data type definitions	**4**	**Lab 6**: VHDL parameterized register file with hierarchical modeling and test bench for design verification
8	VHDL FSM modeling and simulation	**5**	**Lab 7:** VHDL hierarchical modeling, simulation and synthesis of manually controlled display system
9	PicoBlaze microcontroller architecture, operation, instruction set.	**9**	**Lab 8:** PicoBlaze programming, simulation & synthesis
10	Computer input/output functions. **Test #2**	**9**	**Lab 9:** Interfacing external devices to PicoBlaze via input/output ports
11	Programmable logic arrays, programming technologies and interfaces	**3**	**Lab 10:** Interfacing external devices to PicoBlaze via interrupt-driven input/output
12	FPGA and PLD/CPLD architectures and operation	**6**	**Lab 11:** VHDL hierarchical modeling, simulation and synthesis of PicoBlaze controlled display system
13	Introduction to Verilog	**-**	**Lab 11:** conclusion
14	Verilog Examples	**10**	
16	**Final Exam: Thursday, May 2. 2019, 8:00-10:30 a.m.**		

Typical methods for evaluating student performance:

Hour quizzes (2)	40%
Final exam	20%
Lab projects	40%

Computer usage: VHDL modeling, simulation, and synthesis assignments will require the use of Mentor Graphics *Modelsim* and *Xilinx Vivado* computer-aided design (CAD) tools. Some information regarding these tools is available on the ELEC 4200 class web page link listed above. Designs will be downloaded and tested on Digilent/Xilinx Nexys4-DDR FPGA development boards.

Laboratory Assignments: All laboratory exercises are to be done individually. Each lab will be graded as described in the *ELEC 4200 Digital System Design Lab* document. Lab assignments (pre-lab and lab reports) and projects must be turned in on or before the designated date/time to receive credit. Pre-lab assignments will be checked at the start of each lab session. Lab reports are due at the beginning of the lab session following the scheduled date for that lab exercise.

Guidelines and format for lab reports: The required content and format of the lab reports is contained in the *ELEC 4200 Digital System Design Lab* handout, posted on the course web page.

Academic Honesty Policy: All portions of the Auburn University student academic honesty code (Title XII) found online at http://www.auburn.edu/academic/provost/academicHonesty.html apply to this class.

Each student is expected to do his/her own laboratory project. Discussion of various aspects of the project with fellow students is acceptable, provided that designs are not copied. Copied work will be considered a violation of the academic honesty code, and dealt with accordingly.

Class attendance: Students are expected to attend class regularly and on time as indicated by the Auburn University "Policy on Class Attendance". In case of absence, the student is responsible for all course business conducted in class. Make-up exams will be scheduled for excused absences covered by Paragraph 4 of the AU "Policy on Class Attendance".

Policy on unannounced quizzes: There will be no unannounced quizzes.

Accommodations: Students who need accommodations should initiate the process by first making an appointment with The Program for Students with Disabilities, 1244 Haley Center, 844-2096 (V/TT).

Contribution of course to meeting the professional component

Engineering topics: 3 credits
33% engineering science (1 credit)
67% engineering design (2 credits)

Primary program outcomes related to this course:

Graduates will have achieved and demonstrated

(a) an ability to apply knowledge of mathematics, science, and engineering

(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

(g) an ability to communicate effectively

(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Prepared by: V. P. Nelson Date: January 9, 2019