

Adopting Multi-Valued Logic for Reduced Pin-Count Testing

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Abstract—The reduced pin-count test (RPCT) has been proposed for testing cost reduction in various scenarios like scan, test compression and multi-site test. In this paper, we propose a new RPCT technique in which several digital signals are combined into a single multi-valued logic (MVL) signal. Mixed-signal components, digital-to-analog and analog-to-digital converters, are used to compress the tester channels and then to expand the test at the circuit under test. The method allows greater bandwidth efficiency than the existing SerDes alternative. However, the MVL signal can be sensitive to noise and nonlinearity errors. To ensure the reliability of test application, we provide an error control scheme. The paper gives theoretical analysis as well as experimental evidence.

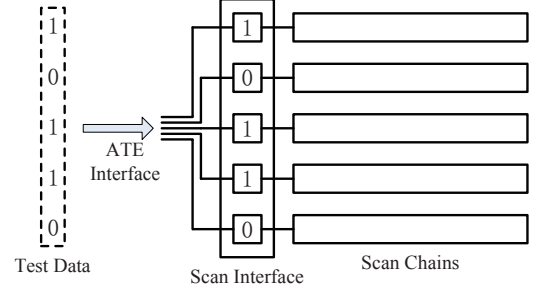
Keywords: Digital test, multi-value logic (MVL), reduced pin-count test (RPCT), tester channel reduction.

I. INTRODUCTION

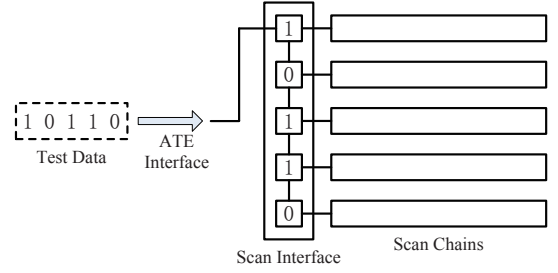
Rapidly increasing testing costs have a fixed component due to expensive automatic test equipment (ATE) and a variable component due to high test time per device under test (DUT) [8]. The key to cut ATE based testing cost is to shorten test time for each DUT and to test more DUTs during same time. Test compression technology tries to shrink the test data volume while retaining the critical information to get the same test coverage. In the simplest form compression methods squeeze out don't-care bits [20]. Some commercially available compression techniques have been able to shrink test size down by 100X.

Multi-site test [22], [23] increases the test throughput and saves testing cost for individual DUT by testing several chips in parallel. Additionally, reduced pin count test (RPCT) helps achieve higher parallelism in multi-site testing [7], [11], [13]. There have been efforts to create new test access mechanisms (TAM) and on-chip design-for-testability (DFT) structures to support RPCT [9], [10], [17], [18], [24]. Most of these employ serializer-deserializer (SerDes) hardware and bandwidth matching technology. A SerDes allows time multiplexing of a test channel [17], [18] and a pin-limited mode can be integrated with test compression scheme [10]. The use of a SerDes with Mentor's embedded deterministic test (EDT) is an example of such a test scheme [9].

Figure 1(a) shows a traditional way to apply test data in which multiple test channels feed into an equal number of scan chains. In pin-limited solutions 1(b), a single test channel feeds test data into multiple scan chains, serially. The test data is serialized in the ATE and deserialized in DUT. Such schemes provide a way to match the bandwidth between ATE and the DUT [9], [23]. However, a serious



(a) Traditional Test Application Method



(b) Pin-limited Test Application Method

Fig. 1: Traditional and pin-limited test application methods.

limitation exists in the SerDes pin-limited solution since it requires the DUT scan speed to be multiple times slower than the ATE channel speed. In cases where the internal scan speed is the same as test channel speed, the test channel speed becomes a bottleneck for test application. For example, in recent work [9], authors assume that an ATE has a speed up to 8 times that of the DUT scan. But when the DUT scan speed is on the order of hundred MHz, the speed requirement for ATE becomes tremendously high, otherwise the scan speed of DUT must slow down. Actually, this problem exists in all existing SerDes based solutions. This requirement sets a limit on the ability to increase test data throughput of a limited number of test channels. To provide high data rate on limited test channels, we propose a novel multi-level logic (MVL) test application method, which can send multiple data bits on a single test channel. We can thus conduct a test with reduced number of test channels. Besides, this method does not conflict with the SerDes solution and can combine with it for more compact test access mechanism (TAM).

In Section II, We give a structural view of our test application method. Considerations on how to determine the detailed design are given in this part. In Section III,

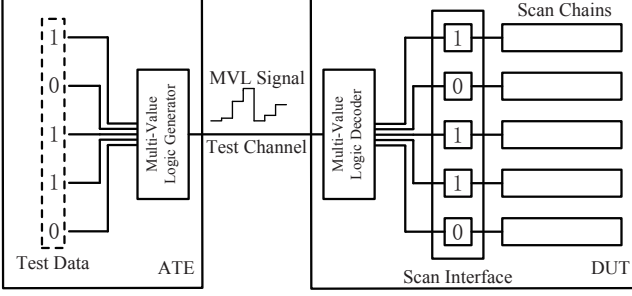


Fig. 2: Overview of multi-valued logic test application.

we discuss the potential transmission errors in the MVL scheme and propose solutions to protect the test application against those. In Section IV, we demonstrate the new idea with a prototype experiment. In Section V, we use a mathematical model to assess the benefits and discuss the overhead. Section VI concludes this work with suggestions for the future.

II. MULTI-LEVEL LOGIC TEST APPLICATION

Originally, the multi-valued logic (MVL) technology was developed to economize the circuit structure by using compact computing elements [16], or to enhance memory capacity by storing more bits in a single memory cell [14]. Although a pure MVL system is still a topic of research, the concept of MVL has been successfully applied to base-band digital data communication and storage. For example, pulse amplitude modulation (PAM) adopts multiple voltage amplitudes to increase the data rate [19]. For the purpose of saving test time and test resources, the MVL will have the benefit of increased data rates. In the chapter “Test and Test Equipment” of International Technology Roadmap for Semiconductors (ITRS) 2011 Edition [6], test application using MVL signal is mentioned as the “second long term test challenge”, which motivated us to conduct this work. A possible rival solution is convert test channel into SerDes link with multiplied clock speed, which is achieved by integrating SerDes transceivers in ATE and DUTs. Compare two solutions, MVL channel has several major advantages: 1. MVL channel uses the same clock with DUTs which voids dealing with different clocks and timing issues; 2. MVL signal consume much less power on the test channel with equal data rate; 3. MVL signal has fewer high frequency parts in terms of frequency response, which relaxes the requirements on test fixture hardware, wiring, etc.

Although the current digital ATE in industry does not generate MVL signals, research toward this goal has been conducted. Advantest [12] has proposed an ATE interface with capacity to generate 16Gbps 4-PAM signal for ethernet interface testing. In our scheme, we do not need such high speed but require more levels. Figure 2 shows an MVL test application structure. An MVL generator in ATE converts multiple digital bits into a single MVL signal. An MVL decoder in DUT converts it back into digital bits and feeds them into the test structure (multiple scan chains in the figure). An N -bit DAC (digital-to-analog converter) and

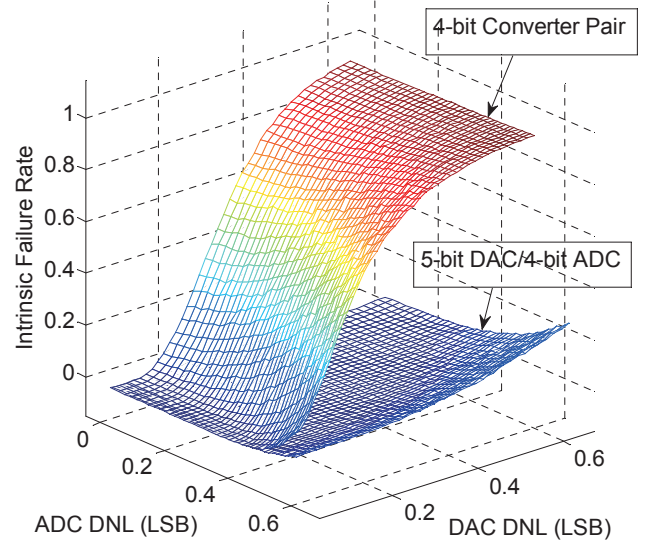


Fig. 3: Intrinsic failure rate vs. ADC/DAC nonlinearities with/without extra resolution.

N -bit ADC (analog-to-digital converter) are used as MVL signal generator and decoder. For ATE, a DAC is added per test channel and test data are sorted into N -bit slices accordingly. In the DUT, an ADC is inserted as the multi-valued logic decoder. The decoded bits are fed into scan chains or decompressor in case of a compression scheme. Because DAC is integrated with ATE, we can have it well calibrated to maintain high accuracy. The ADC integrated in DUT has limitations on area and power consumption and as a result its accuracy may be compromised.

III. RELIABILITY ANALYSIS AND PROTECTION SCHEME

An MVL signal level can be a small fraction of the peak magnitude and hence reliability issues are more stringent than those for binary signals. We define this reliability problem as either an *intrinsic failure* or a *noise-induced error*.

A. Intrinsic Failure and Protection

Data converters have nonlinearities. The output of DAC and code ranges of ADC may deviate from ideal, which will possibly cause permanent misinterpretation in a matched converter pair. We define this situation as *intrinsic failure*. To have no intrinsic failure, the output $V(n)$ of DAC should be set in the range for the n th code of ADC as:

$$\begin{aligned} V_{out}(n) &\in \{V_{ref}(n-1), V_{ref}(n)\}, n \in \{1, 2^N - 2\}; \\ V_{out}(0) &\in \{-\infty, V_{ref}(0)\}; \\ V_{out}(2^N - 1) &\in \{V_{ref}(2^N - 2), +\infty\}. \end{aligned} \quad (1)$$

where V_{out} is output voltage of DAC, V_{ref} is the reference voltage of ADC. If a data converter pair violates equation (1), we call this an intrinsic failure. We use a statistical model based on a 4-bit converter pair to illustrate how data converter accuracy effects intrinsic failure rate. The result is shown in Figure 3. We observe that the intrinsic failure rate increases as digital nonlinearity (DNL) of ADC/DAC increases. Thus, DNL should be small to keep intrinsic failure

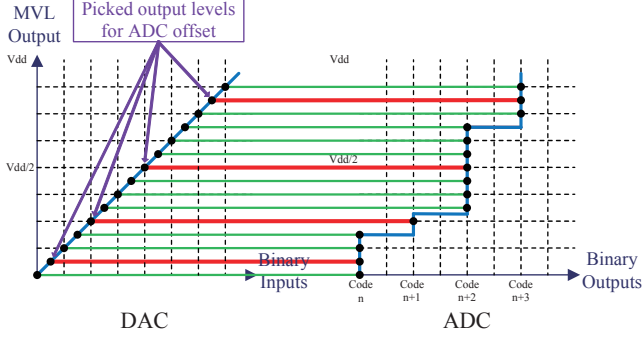


Fig. 4: Communication between fine-resolution DAC and coarse-resolution ADC.

rate low. This makes the cost of ADC/DAC integration high for good performance.

It is reasonable to assume that we will have better control on DAC nonlinearity. Therefore, we developed a scheme to calibrate ADC nonlinearity by manipulating the DAC outputs, which successfully eliminates intrinsic failures. Figure 4 illustrates how this works: N_{extra} additional bits in DAC enable it to generate much finer output levels, which reduce the effect of DAC nonlinearity to $\frac{1}{2^{N_{extra}}}$. Also, this finer output capability can be used to offset the on-chip ADC nonlinearity. As Figure 4 shows, the transfer function of ADC has unequal steps which turns out to be nonlinearity. The step height of code $n + 1$ is extremely short, which will probably cause intrinsic failure: The DAC output for code $n + 1$ falls out of this small range. If we pick the marked DAC output from the finer output levels, intrinsic failures are avoided. In simulation, we use a 5-bit DAC to calibrate the original 4-bit ADC. The result is shown in Figure 3: the intrinsic failure rate is greatly reduced. By the meantime, with ADC nonlinearity being offset, the noise margin will always be maximized. Due to factors like small featuring size, aging and PVT, the ADC performance may fluctuate. Our calibration scheme will always guarantees best matching converter pair for it being done in real-time.

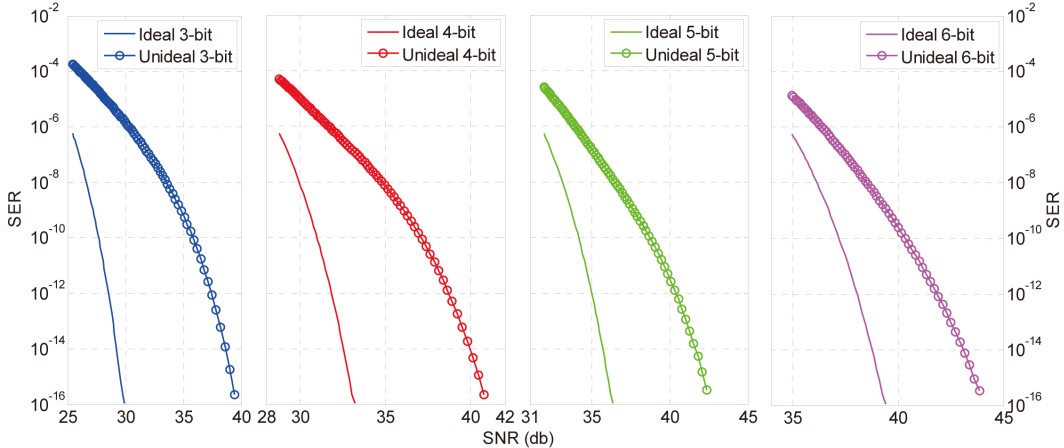


Fig. 5: SER vs. SNR for nonlinear data converters with different resolutions.

B. Noise-Induced Conversion Error and Prevention

We use the signal-to-noise ratio (SNR) of the test channel as a measure of all kinds of noise from which the test application system may suffer, including the noise from test application system, the environmental interference, on-chip digital switching noise, etc. We use symbol error rate (SER) to quantify system reliability against noise. Obviously, higher data converter resolution results in worse noise tolerance for reduced noise margin. If we consider nonlinearities, the noise margin is further reduced, making SER even higher. Next, we simulate to determine how nonlinearities and noise increase SER . The condition for correct test data decoding is,

$$V_{ref}(n-1) - V_{out}(n) < V_{noise} < V_{ref}(n) - V_{out}(n). \quad (2)$$

where V_{noise} is the equivalent noise signal on the test channel. Figure 5 shows the relation between SER and SNR for different converter resolutions, in which ADC/DAC DNLs are 0.2LSB and 0.1LSB, respectively. Compared with the ideal situation, the SER of nonlinear data converters becomes worse.

Given the SER for a DAC/ADC pair, we can estimate the probability that the whole test is applied correctly as: $(1 - SER)^{\frac{T}{R}}$, where T is the number of test data bits and R is the data converter resolution. We call this probability as CAR or *correct application rate*. If the test data is incorrectly decoded, the test result is not credible, which would degrade yield or increase test escapes. We propose an error control scheme to increase CAR and eliminate noise-induced errors. The basic idea in this error control scheme is to treat MVL decoder as another DUT, whose output becomes a new kind of test response. Figure 6 gives the structural view.

The MVL decoder receives the MVL signal and convert it into test data. When the decoded test data are fed into scan chains or test decompressor, they go through the error control circuit at the same time. In our design, the error control circuit is an MISR (multiple-input signature registers) as an additional test response compactor. During test application, the decoded test data are compacted. When the test application is finished, we get a new test response signature in

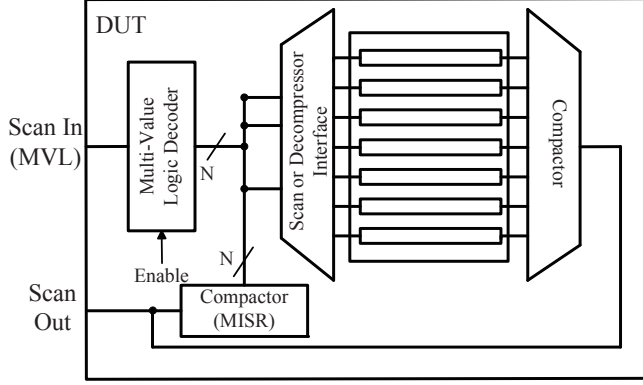


Fig. 6: Test data application interface of DUT with MVL decoder and error control circuit.

error control circuit, namely, applied test signature (ATS). Besides, we still have the traditional test response signature (TRS) from the traditional test response compactor. Figure 7 shows the flow chart of the test procedure with ATS and TRS. In the first step, the ATS is examined to make sure the test data is being correctly applied. Following that, the TRS is examined to check whether the DUT passes the test. But, if the ATS does not pass the first step (signature aliasing is ignored), we require it to be retested. In such a case, the correct application rate with error control $CAR_{ec} = 1 - (1 - CAR)^{N+1}$, where CAR is the original correct application rate and N is the maximum retest times. The incorrect test application rate is suppressed by the power of retest times. We can equivalently consider the system SER is lowered as a tradeoff for error control circuit area and extra retest time. The implementation of error control circuit is not a problem for it is a well developed technology.

IV. PROTOTYPE TESTING IMPLEMENTATION AND RELIABILITY MEASUREMENT

To demonstrate the effectiveness and reliability of our scheme, we developed a simulation hardware platform based on NI ELVIS II+ [5] (National Instruments Electronic Virtual Instrumentation Suite II+). Commercially available 8-bit DAC AD557 [1] ($DNL \pm 0.5LSB$) and 8-bit ADC AD7822 [2] ($DNL \pm 0.75LSB$) are used as MVL generator and decoder, respectively. Similar to [21], our test data and configuration are programmed with Labview [4] in PC, and sent to ELVIS prototype board through USB connection. Any test responses are captured by the prototype board too.

A. Reliability Measurement

In this phase, we try to simulate:

- ATE sending MVL test signal: Pseudo-random test patterns are generated by Labview program and sent to the MVL generator AD557 on the prototype board.
- DUT decoding MVL signal: The output of AD557 feeds into MVL decoder AD7822. The outputs of AD7822 are wired back to prototype board for response capture.

The hardware setup for SER measurement is shown in Figure 8. The measurement test runs at 0.4MHz due to

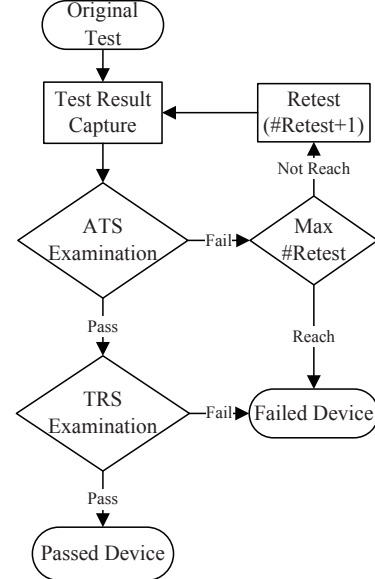


Fig. 7: Flowchart of test procedure with applied test signature (ATS) and test response signature (TRS).

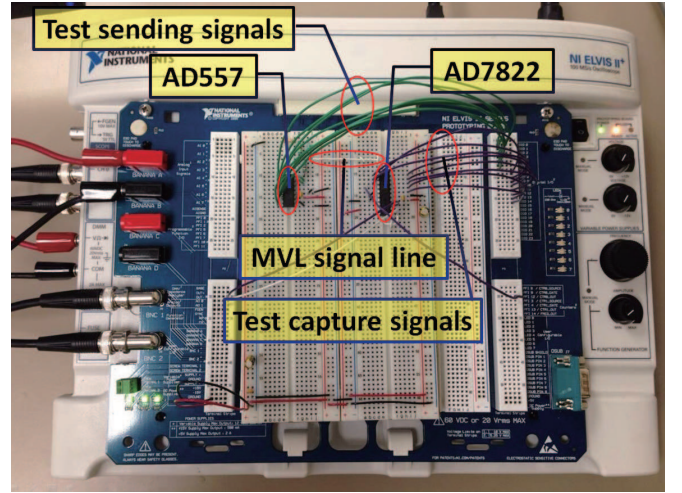


Fig. 8: Test setup for symbol error rate (SER) measurement with NI ELVIS II+ and data converters.

hardware speed limitation. The Labview program compares the original test data and the captured decoded data to calculate the decoding SER . A voltage divider at the output of the MVL generator changes the full scale voltage of MVL signal, which gives different noise margins. The noise margin is calculated as $\frac{V_{fullscale}}{2^{bit+1}}$. We show the relationship between SER and noise margin in Figure 9, which contains two sets of measured data: 1) FPGA connected, 2) FPGA not connected. Both cases fit well with the Gaussian noise error function. We observe that SER gets worse with FPGA-induced digital noise. We did not measure SER below 10^{-10} for the slow clock speed. However, we can still predict SER from fitted curves in Figure 9.

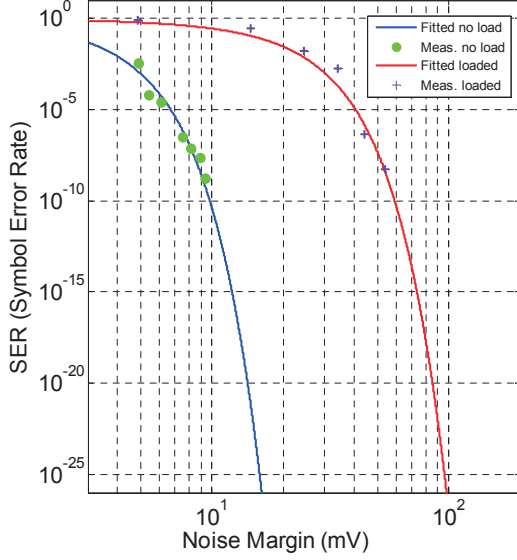


Fig. 9: SER vs. noise margin in prototype implementation.

B. Calibration of Data Converter Nonlinearities

In Section III, we proposed a calibration method to overcome the nonlinearity problem. Here we conduct a calibration experiment with the prototype system to show the benefit. First, we pick 32 arbitrary output codes from AD577 to emulate a nonlinear 5-bit DAC, and then follow it up with an emulated nonlinear 5-bit ADC. We conducted an *SER* measurement, which gave a value 1.88×10^{-2} . Next, we apply our calibration algorithm to the DAC, reassigning the output codes to offset the ADC nonlinearities. This time we measured the *SER* as 1.01×10^{-7} , which is an improvement by five orders. This proves the calibration to be meaningful.

C. Scan Test of an Altera DE2 [3] FPGA DUT

Now, we simulate a typical scan test behavior. The ELVIS system with AD577 is used as an MVL signal compatible ATE and DE2 FPGA board with AD7822 work as the MVL signal compatible DUT in Figure 10. Benchmark circuit s298 with scan structure inserted is burnt into DE2 FPGA board. We group five inputs (*/G0*, */G1*, */G2*, */scan_in1*, */scan_en*) to be sent in MVL format. The other two inputs are left in binary mode because */blif_clk_net* is the test clock coming from the ATE (prototype board); and the */blif_reset_net* stays 0 during the whole test. Labview program captures the decoded test data and the test response. The test result is the same as that of traditional test, but only uses one MVL signal line in place of five binary signal lines.

V. PERFORMANCE AND OVERHEAD

The data rate of a traditional binary data transmission channel equals the ATE channel frequency. In our method, the data rate of test channel is ATE channel frequency multiplied by the ADC resolution. However, retesting DUTs costs extra test time, this equivalently reduces the average data rate. Assuming that the correct application rate is *CAR*, resolution is *R* and the maximum retest time is *N*,

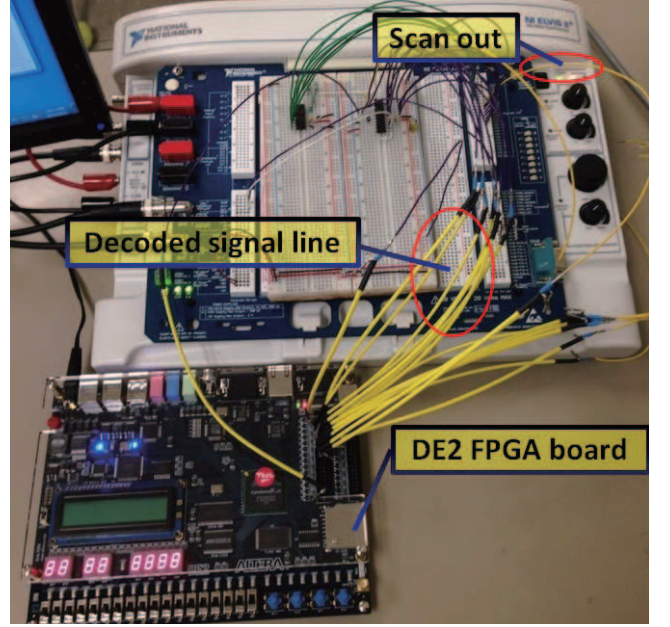


Fig. 10: Test setup for scan test applied by NI ELVIS II+ data converters to a DUT implemented on DE2 FPGA board.

TABLE I: Maximum *SER* for different test data volume and resolution to reach 90% *CAR*.

$T(\text{bit}) \backslash R$	3	4	5
10^6	3.16×10^{-7}	4.21×10^{-7}	5.27×10^{-7}
10^8	3.16×10^{-9}	4.21×10^{-9}	5.27×10^{-9}
10^{10}	3.16×10^{-11}	4.21×10^{-11}	5.27×10^{-11}
ϕ	2.7	3.6	4.5

we can get the ratio between average MVL channel data rate and binary channel data rate as:

$$\phi = \frac{R}{[(N+1)(1-CAR)^{N+1} + CAR \sum_{n=1}^{N+1} n(1-CAR)^{n-1}]} \quad (3)$$

$$= \frac{R \cdot CAR}{1 - (1-CAR)^{N+1}}.$$

A sample case demonstrates the benefit of this scheme. Assume that the maximum retest time is 4 and we require at least 99.999% DUTs receiving correct test data within maximum time of retest. Then *CAR* needs to be no less than 90%, which determines the maximum *SER*s with different test data sizes, shown in Table I.

Associated with *SER* data of FPGA loaded case in Figure 8, we can get the minimum noise margin and full scale voltage requirement for each case from Table I. If there is a maximum 1.5V full scale voltage constraint on MVL signal pin, then we can have test data rate increased by 2.7 times for test data size from 10^6 to 10^{10} with 3-bit data converters, and 3.6 times for test data size 10^6 with 4-bit data converters. Other cases exceed the constraint. Notice that this *SER* data is measured in a noisy environment, which means

TABLE II: Minimum noise margin and full scale voltage for each case in Table I.

43.9mV / 702.4mV	43.4mV / 1388.8mV	46.9mV/3001.6mV
51.3mV / 820.8mV	50.8mV/1625.6mV	50.5mV/3232mV
57.8mV / 924.8mV	57.4mV/1836.8mV	57.1mV/3654.4mV

the full scale voltage requirement will be smaller in a real test situation so that better improvement can be expected.

The overhead here includes an on-chip MVL decoder and an MISR. The MISR takes small area which may be ignored. The on-chip decoder seems to be area consuming as an ADC. Nevertheless, the complexity of ADC grows exponentially with its resolution, so that a small resolution ADC still produces impressive improvement (even a 2-bit ADC doubles the data rate) without taking too much area. Moreover, we propose this technique for pin-limited situations, which minimizes the number of required ADCs. Also, if the DUT has integrated ADCs (like many mixed-signal ICs), then those can be used as MVL decoders with no extra cost. As technology advances, we observe that ADC designs [15] for data communication show greater economy of area and power, leading us to believe that we will be able to control the overhead and power of the MVL application to remain under acceptable limits in the future.

VI. CONCLUSION AND FUTURE WORK

This is the first proposal of digital test application using the mixed-signal technology. The data rate scales up with on-chip ADC resolution and the method saves test channels or shortens test time. We also expose the factors that may lead to test application failure and provide remedies.

Aside from the theory and experiment presented, there is works in progress that will involve demonstration with a real tester. It will be beneficial to develop further applications of the MVL technique. A possible direction for future investigation will be to combine the MVL and SerDes approaches in various test data compression schemes.

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